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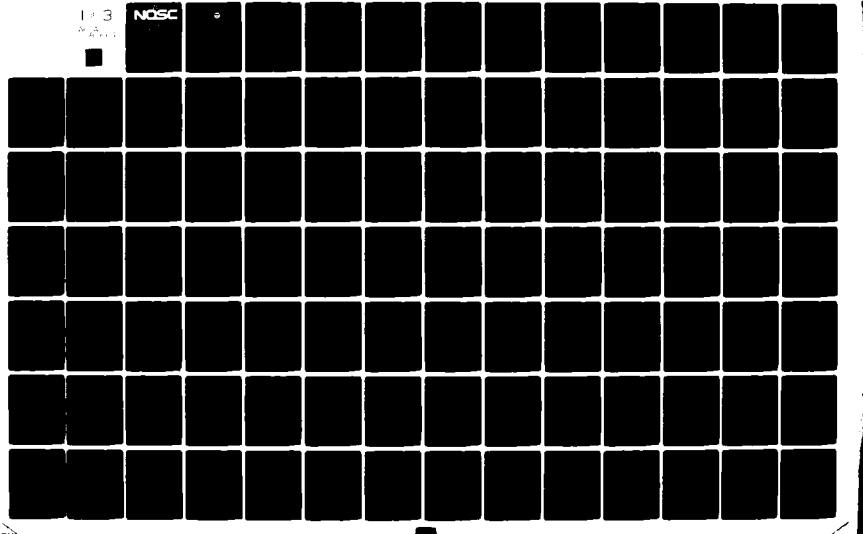

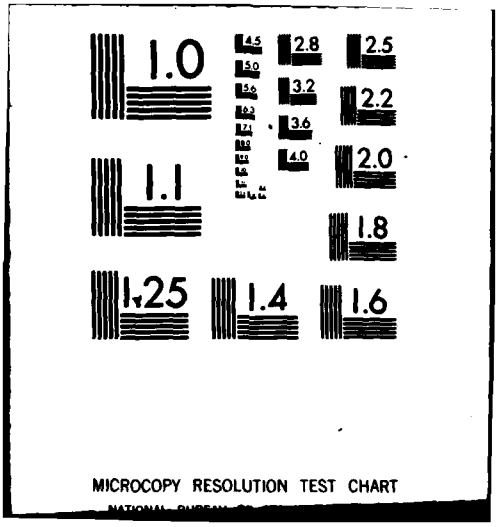
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HIGH FREQUENCY ANALOG LSI DEVELOPMENT

Second Annual Interim Report

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(TRW)

12 November 1979

Interim Report: 1 September 1978 — 12 November 1979

Prepared for
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NAVAL OCEAN SYSTEMS CENTER
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IF amplifier	Current source	Double-to-single converter	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report documents all design and related analysis efforts undertaken in the second year of a three-year program aimed toward utilizing OAT fabrication technology to develop building block circuits which satisfy the system requirements of communication networks operating through L-band signal frequencies. The designs of a wideband RF amplifier, narrowband IF amplifier, four-quadrant analog multiplier, wideband operational amplifier, and high frequency voltage

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controlled oscillator are discussed at considerable depth, and the available experimental characterizations of these units are documented. As a prelude to circuit design discussions, the theories of bandwidth estimation, RF power flow, stability, and interstage coupling are rigorously developed and explained. These theories form the foundation upon which the circuit design methodology is structured.

OBJECTIVE

Use oxide-aligned transistor (OAT) fabrication technology to develop circuit techniques and building block circuits which satisfy the system requirements for communication networks operating at signal frequencies through L-band.

RESULTS

1. The GPS1 and GPS1A test chips have been fully characterized. Their performance has been found to be poor due to low RF amplifier gain and the presence of spurious frequencies within the code tracking loop. The RF amplifier gain is low due to inappropriate inter-stage matching incurred as a result of ostensibly uncontrollable on-chip inductor parasitics. Code tracking loop oscillations are present in most GPS1A chips due to an improperly stabilized operational amplifier.

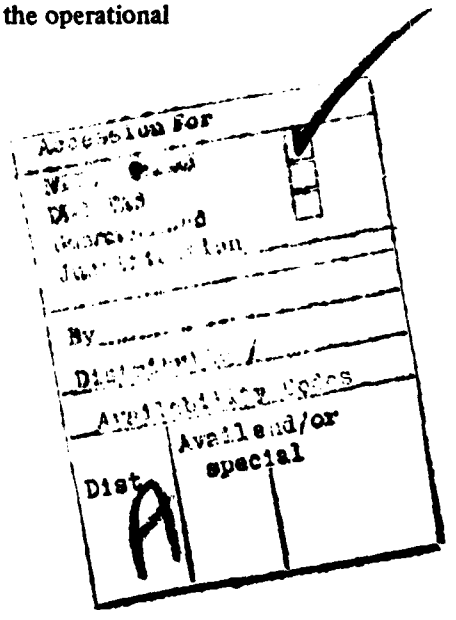
2. RFCS-1 is undergoing test and evaluation. Preliminary results portend excellent RF and IF amplifier performance which closely tracks with analytical predictions documented at the conclusion of the circuit design phase.

RECOMMENDATIONS

1. Complete the characterization of RFCS-1.

2. Based upon experience gained through development of RFCS-1, design, fabricate and test a Costas Loop demodulator using the completed RFCS-1.

3. Evaluate the feasibility of stand-alone RFCS-1 building blocks using the operational amplifier and analog multiplier circuits as test vehicles.



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1.0 INTRODUCTION

In September of 1977, TRW DSSG undertook a three-year program to use oxide aligned transistor (OAT) fabrication technology to develop circuit techniques and building block circuits appropriate to the satisfaction of system requirements for communication networks operating at signal frequencies through L-band. The program, sponsored by the Naval Electronic Systems Command and directed by the Naval Ocean Systems Center, under Navy Contract N000123-77-C-1045, is configured in terms of six distinct tasks.

The object of Task 1 is to develop analog circuit design methodologies which efficiently exploit OAT monolithic processes. In Task 2, a GPS receiver system interface study is performed, and a complete GPS receiver is configured. This system configuration exploits the RF building block circuits developed and fabricated as an implicit part of Task 3. In Task 4, a GPS receiver chip is actually fabricated, and in Task 5, additional RF building block circuits are developed and fabricated. These additional circuits include an RF amplifier, three types of voltage-controlled oscillators, an RF switch, an IF amplifier, a four-quadrant analog multiplier, and a high speed operational amplifier. The final phase of the program, Task 6, addresses the design of a Costas demodulator, explores a variety of advanced circuit concepts, and demonstrates the plausibility of utilizing OAT RFLSI methodology in the realization of stand alone building block circuits that can be used in a broad variety of electronic system applications. The final task also examines the suitability of OAT RFLSI to military communication applications.

From September 1977 through August 1978, contractual efforts centered largely around Tasks 1, 2, 3 and 4 and accordingly, the cognate results of these efforts are reported in the first Yearly Interim Report, which was filed with the Navy in October 1978. From September 1978 through August 1979, the testing aspects of Task 4, as well as both the design and partial testing of circuits implicit in Task 5 received major

attention. Additionally, the Microelectronics Center (MEC) of TRW DSSG spent a limited amount of time exploring a few advanced circuit design concepts and examining circuit candidates suitable for implementation as stand-alone building block configurations. This report concentrates on only the latter of the foregoing tasks; that is, it deals with contractual efforts expended in the time frame September 1978 through August 1979.

2.0 THE YEAR IN REVIEW

The engineering research and development work performed during the second year of contract performance can be codified into four distinct work packages. These are (1) circuit design theory, (2) circuit development, (3) testing, and (4) building block fabrication.

Section (3.0) of this report addresses the first area of work, circuit design theory. The concept of a dominant pole response is exploited to develop circuit bandwidth estimation techniques that can be straightforwardly utilized in the course of a network design exercise. Although neither the pole dominance concept nor the analytical technique pertaining to bandwidth estimation is new to circuit theory, the application of the concept to the problem of ascertaining device quality in an RFLSI environment constitutes a pathfinding endeavor.

Additional original research in circuit design theory can be claimed with respect to optimizing the performance of amplifier interstaging through use of an inductively peaked active load. The optimized design criteria accounts for finite bandwidth in the driver stage, as well as finite poles in the driving point characteristic of the driven stage.

Section (3.0) also includes a discussion of two-port network theory, as applied to the task of developing and implementing prudent RFLSI design methodology. To this end, the indirect use of measured scattering parameters to design and analyze generalized RFLSI configurations receives considerable attention.

Section (4.0) explicates the new circuits developed over the past year. Included in the list is a negative resistance gain cell, which is suitable for use in applications which require extremely high gain over a moderately broad passband, a number of active current sources that are capable of sustaining high driving point magnitude of impedance over wide frequency ranges, a differential-to-single-ended converter that utilizes only npn devices, and a Darlington configured level

shifter capable of realizing very low output impedance through L-band frequencies. The section concludes with a reexamination of the thermal stability problem in a voltage reference circuit proposed in an earlier phase of contract work.

Section (5.0) pertains to the design and fabrication of RFCS-1, which is a set of six (6) electronic building blocks focused upon as an implicit part of Task 5. RFLSI design philosophy is adequately exemplified through documentation of the design methodology for three of the six fabricated circuits.

The second year of contract efforts might very well be remembered subsequently as the year in which massive strides were taken to mature the genuinely challenging discipline of analog high frequency testing. In Section (6.0), test results pertinent to the original GPS chip and the reprocessed GPS chip (known as the GPS1A) are reported.

Section (7.0) concludes the report by summarizing work performed at this juncture, delineating status, and offering thoughts on future work commensurate with maturation of RFLSI technology. To the latter end, the feasibility of network gyration as a tool for monolithic realization of inductance characteristics is postulated.

3.0 CIRCUIT DESIGN THEORY

3.1 Bandwidth Estimation [1]

A pressing concern of engineers confronted with the task of designing wideband linear amplifiers is the ability to calculate the bandwidth that can be realistically expected of a proposed circuit design before the design proposal is committed to monolithic fabrication. In general, there is no compelling need to predict bandwidth precisely; rather, estimation of a realistic lower or upper limit of physically realizable bandwidth is more germane to pragmatic circuit design issues. To this end, a number of reasonable approximations can be exploited.

First, it is normally desired that the transfer function of a wideband amplifier display lowpass response characteristics at all signal frequencies in the passband of interest and up to an immediate neighborhood of the upper half power frequency. A sufficient, but not necessary, set of conditions commensurate with this desire is that the circuit poles be real and that the circuit zeros, if any, have magnitudes that greatly exceed the magnitude of the lowest frequency pole. For reasons of stability, all circuit poles must lie in the open left half of the complex frequency plane, but zeros may lie in either left or right half planes. Second, it is assumed that adjacent real poles are widely separated in the complex frequency (or s-) plane. This assumption is not a prerequisite to bandwidth estimation abilities, but when coupled with the third and final assumption, it substantially facilitates all cognate computations. The third assumption is that capacitors are the only elements capable of energy storage in the considered or proposed design. This constraint precludes application of the forthcoming estimation theory to inductively coupled networks or to networks whose response in the frequencies of interest are significantly influenced by parasitic inductances in series with designable branch elements.

3.1.1 Time Moments

In accordance with the above discussion, the transfer function, say A(s), of a given circuit proposal reads

$$A(s) = \frac{A_o}{(1 + s/s_1)(1 + s/s_2) \cdot \cdot \cdot (1 + s/s_N)} , \qquad (3\text{-}1)$$

where s is the complex frequency variable, the N poles of the circuit are located in the s-plane at $s = -s_1$, $s = -s_2$, $\cdot \cdot \cdot$, $s = -s_N$, where each of the s_k are real numbers, and A_o is the low frequency or "DC" circuit gain. An expansion of the denominator on the right-hand side of (3-1) produces the equivalent form,

$$A(s) = \frac{A_o}{1 + b_1 s + b_2 s^2 + \cdot \cdot \cdot + b_N s^N} , \qquad (3\text{-}2)$$

where all b_k are positive real numbers.

If (3-1) is taken as representative of a broad class of lowpass linear active networks, the first network time moment is defined to be

$$T_1 = \sum_{k=1}^{N} \frac{1}{s_k} . \qquad (3\text{-}3)$$

The second time moment, T_2, is gleaned from the expression

$$T_2^2 = \sum_{k=1}^{N} \frac{1}{s_k^2} , \qquad (3\text{-}4)$$

and in general, the mth time moment derives implicitly from

$$T_m^m = \sum_{k=1}^{N} \frac{1}{s_k^m} . \tag{3-5}$$

From (3-1) and (3-2), it is immediately clear that

$$b_1 = T_1 \tag{3-6}$$

and

$$b_2 = \sum_{\text{all } k<j} \left(\frac{1}{s_k s_j}\right). \tag{3-7}$$

The last expression is equivalent to

$$b_2 = \frac{1}{2}\left\{\left[\sum_{k=1}^{N} \frac{1}{s_k}\right]^2 - \sum_{k=1}^{N}\left(\frac{1}{s_k^2}\right)\right\} \tag{3-8}$$

and by virtue of (3-3) and (3-4),

$$b_2 = \frac{1}{2}(T_1^2 - T_2^2). \tag{3-9}$$

Since a stable system implies b_2 (and all other b_k) in (3-2) are positive, (3-9) suggests that $T_1 > T_2$. In similar fashion, it can be shown that

$$b_3 = \frac{1}{3}\left[T_3^3 + \frac{1}{2} T_1(T_1^2 - 3T_2^2)\right] \tag{3-10}$$

and in general, b_k is always expressible in terms of the first k time moments.

The time moment concept is a convenient vehicle for the formulation of three analytical methods of bandwidth estimation in a lowpass system. More correctly, the analytical techniques developed herein are applicable to problems involving the computation of the upper 3-dB cutoff frequency which, in a wideband lowpass system, is nominally equivalent to system bandwidth, say B.

The first of the aforementioned techniques evolves if a consideration is made of the special case of widely separated amplifier poles; that is,

$$s_1 << s_2 << s_3 << \cdots << s_N. \tag{3-11}$$

If the lowpass system defined by (3-1) satisfies (3-11), (3-5) verifies that all m-time moments for the considered system are virtually identical and more specifically,

$$T_1 \approx T_2 \approx T_3 \approx \cdots T_m \approx \frac{1}{s_1}. \tag{3-12}$$

But if $T_1 \approx T_2$, b_2 in (3-9) vanishes, $T_1 \approx T_2 \approx T_3$ renders approximately zero value for b_3 in (3-10), and by inductive reasoning, (3-12) is seen to imply $b_k \approx 0$ for $k = 2, 3, 4, \ldots N$. Thus, the transfer function of a lowpass structure possessed of only widely separated poles reduces to the simplified form,

$$A(s) \approx \frac{A_0}{1 + b_1 s}. \tag{3-13}$$

It is apparent that the 3-dB bandwidth, say B_w, of such a structure is

$$B_w = \frac{1}{b_1} \tag{3-14}$$

or equivalently,

$$B_w = \frac{1}{T_1} . \tag{3-15}$$

Equation (3-15) is a quantitative statement of the obvious fact that the bandwidth of a lowpass system having widely scattered poles is essentially the frequency of the pole nearest the s-plane origin. A considerably more interesting feature of (3-15) is that it implicitly possesses circuits-oriented practicality. In particular, first time moment T_1 can be obtained directly, often by trivial computation, from the linearized amplifier model. Before proceeding with the development of this notion, it is wise to offer a somewhat philosophical discussion of the shortcomings inherent in (3-15).

The most important point to be made in regard to the preceding is that the bandwidth of a lowpass amplifier approximates the inverse of the amplifier first time moment <u>if and only if the high frequency poles are widely separated in the s-plane</u>. It is especially appropriate to recall this assertion in a forthcoming discussion which puts forth a computational algorithm for T_1 that is valid for <u>any</u> amplifier, regardless of the nature of its pole conglomeration. Since it is generally impossible to predetermine the geometric pole pattern of a given amplifier, the aforementioned algorithm, being insensitive to pole pattern, is a convenient analytical tool. But (3-15) is a function of pole density and thus blind employment of the result in question can conceivably lead to intolerable errors.

As a means of dramatizing the foregoing assertion, consider an amplifier containing an Nth order real pole at $s = -s_o$. Such a configuration, which is certainly in blatant violation of the wide separation constraint, is characterized by the transfer function,

$$|A'(s)| = \frac{|A'_o|}{(1 + s/s_o)^N} . \tag{3-16}$$

The true bandwidth, say B, is implicitly defined by the relationship,

$$|A'(jB)| \triangleq \frac{|A_0|}{2^{1/2}}, \tag{3-17}$$

and it follows straightforwardly that for the system of (3-16),

$$B = s_0[2^{1/N} - 1]^{1/2}. \tag{3-18}$$

A considerably different bandwidth result materializes if (3-15) is invoked. Recalling that the first time moment is the sum of the inverse of pole frequencies, T_1 for the problem under consideration is N/s_0, whence

$$B_w = \frac{s_0}{N}. \tag{3-19}$$

Figure (3.1) portrays a superposition of the plots, B/s_0 and B_w/s_0 versus N, together with a graphical delineation of the error incurred through use of (3-19). Note, for example, that the analyst who is blissfully aware that the five poles of his network are identical suffers about a fifty percent error by employing the T_1-method for bandwidth estimation.

It must be remembered that the error plot of figure (3.1) is applicable only to the highly specialized case of an amplifier characterized by an Nth real order pole. In practice, it is unrealistic to presume that a given lowpass amplifier contains a large number of identical poles and hence, it can be conjectured that the error resulting from employment of (3-15) is appreciably less than that which is portrayed graphically. Nevertheless, the theoretical possibility of grossly erroneous results, coupled with inability to predetermine the nature of pole conglomeration, justifies the need to explore other bandwidth estimation measures which either circumvent or neutralize this computational uncertainty.

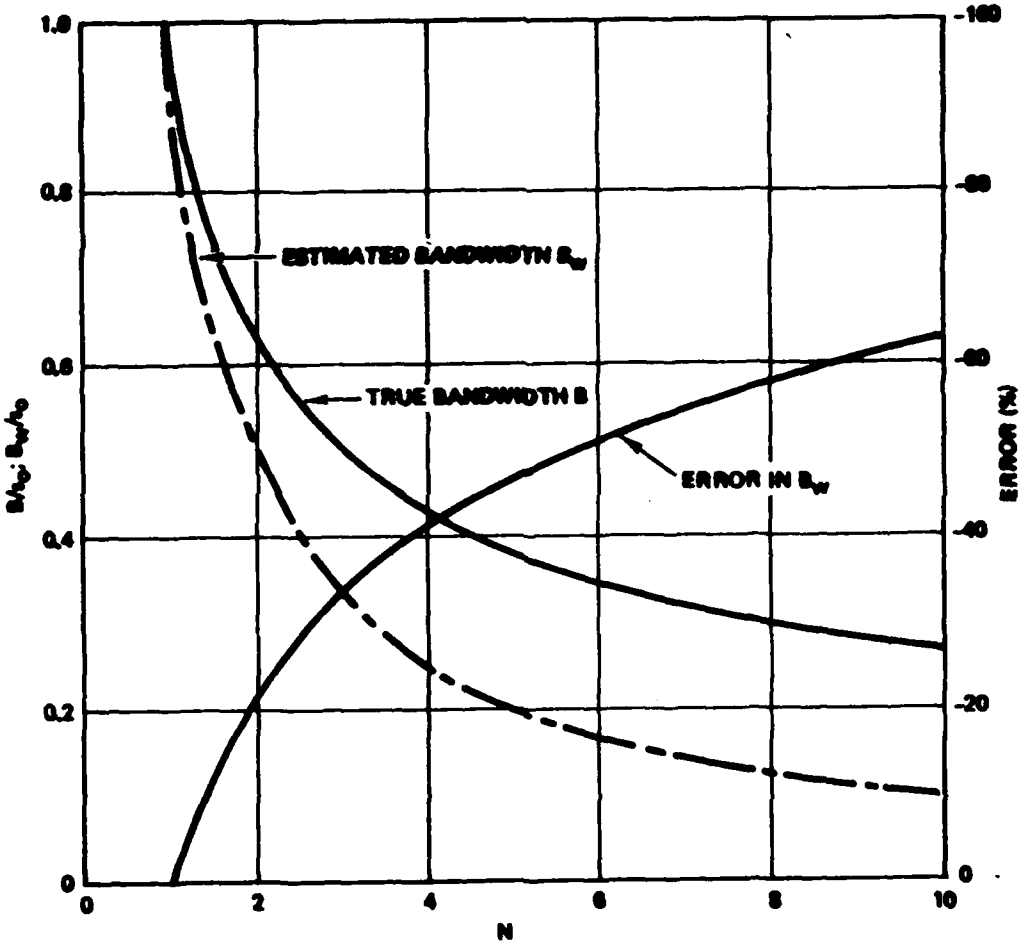


Figure (3.1). Normalized True and Estimated Bandwidths, Along With the Error of the Estimated Bandwidth for an Amplifier Possessing an Nth Order Pole at $s = -s_0$.

Returning to (3-1), it is possible to write

$$\mathrm{Ln}\left[\frac{A(s)}{A_o}\right] = -\mathrm{Ln}(1 + s/s_1) - \mathrm{Ln}(1 + s/s_2) - \cdots - \mathrm{Ln}(1 + s/s_N). \quad (3\text{-}20)$$

If for all k, $|s/s_k|$ is less than unity, an assumption which implies that the immediately ensuing considerations are applicable for only those signal frequencies which do not exceed the smallest of the high frequency pole frequencies, each natural logarithm on the right-hand side of (3-20) can be expanded into a MacLaurin series in s. After appropriate algebraic manipulation, this series is found to be

$$\mathrm{Ln}\left[\frac{A(s)}{A_o}\right] = -\left(\frac{1}{s_1} + \frac{1}{s_2} + \cdots + \frac{1}{s_N}\right)s + \frac{1}{2}\left(\frac{1}{s_1^2} + \frac{1}{s_2^2} + \cdots + \frac{1}{s_N^2}\right)s^2$$

$$- \frac{1}{3}\left(\frac{1}{s_1^3} + \frac{1}{s_2^3} + \cdots + \frac{1}{s_N^3}\right)s^3 + \cdots, \quad (3\text{-}21)$$

and by virtue of (3-5),

$$\mathrm{Ln}\left[\frac{A(s)}{A_o}\right] = -T_1 s + \frac{1}{2}(T_2 s)^2 - \frac{1}{3}(T_3 s)^3 + \cdots . \quad (3\text{-}22)$$

For steady state sinusoidal considerations, (3-22) becomes

$$\mathrm{Ln}\left[\frac{A(j\omega)}{A_o}\right] = -\frac{1}{2}(\omega T_2)^2 + \frac{1}{4}(\omega T_4)^4 + \cdots + j[-\omega T_1 + \frac{1}{3}(\omega T_3)^3 - \cdots]. \quad (3\text{-}23)$$

Since signal frequency is necessarily restricted in accordance with the constraint, $|s/s_k| < 1$, it is reasonable to adopt an analytical procedure which obviates terms in ω involving powers in excess of two. Hence,

$$\mathrm{Ln}\left[\frac{A(j\omega)}{A_o}\right] \approx -\frac{1}{2}(\omega T_2)^2 - j\omega T_1. \quad (3\text{-}24)$$

Clearly,

$$A(j\omega) \approx A_0 EXP[-\frac{1}{2}(\omega T_2)^2 - j\omega T_1] \tag{3-25}$$

and concomitantly,

$$|A(j\omega)| \approx |A_0| e^{-\frac{1}{2}(\omega T_2)^2} \tag{3-26}$$

$$\phi(\omega) \approx -\omega T_1, \tag{3-27}$$

where $\phi(\omega)$ symbolizes the phase response of the considered system.

Equation (3-26) constitutes a mathematical definition of the so-called "Gaussian response" approximation to the frequency function of a lowpass configuration. In more explicit terms, for frequencies not exceeding the smallest pole frequency, the transfer function magnitude of any lowpass structure obeying (3-1) can be approximated by (3-26), provided the approximation necessary to arrive at (3-24) is satisfied. Additionally, a "Gaussian" system is seen to possess linear phase lag or equivalently, constant envelope delay.

The Gaussian approximation is certainly valid for signal frequencies which approach the considered system bandwidth B, since for a lowpass system whose zeros are at infinity, B is always smaller than the smallest critical frequency. Accordingly, the well-behaved function on the right-hand side of (3-26) is a useful pedagogical tool for bandwidth estimation. Employment of the concept underlying (3-17) readily yields

$$B_g = \frac{(Ln2)^{1/2}}{T_2} = \frac{0.833}{T_2}, \tag{3-28}$$

where subscript "g" connotes a result predicated on the Gaussian approximation.

It is conceivable that (3-15) and (3-28) can deliver markedly different bandwidth estimates. This situation, although seemingly unfortunate, is to be expected, since each result is predicated on distinctly different operating circumstances. For example, B_w approximates the true 3-dB bandwidth if and only if all system time moments are approximately equal. On the other hand, (3-28) is spawned by (3-24) which, in turn, is a valid truncation of (3-23) if all time moments above the second are essentially zero. Obviously, the requirement, $T_k \approx 0$ for $k = 3, 4, \cdots m$ precludes a sparse pole population and moreover, it tends to imply a dense pole conglomeration. Semi-quantitative support for the last assertion is available through a reconsideration of the transfer function in (3-16) for which $T_2^2 = N/s_o^2$, whence

$$B_g = \left(\frac{0.833}{N^{1/2}}\right)s_o . \tag{3-29}$$

For the special case of N = 1 (which satisfies the wide separation doctrine), (3-29) delivers a bandwidth estimate that is about 17% lower that the true bandwidth computed from (3-18). For N = 2, this error attenuates to 8%, while N > 4 produces inconsequentially small errors.

Rigorous support for the negligible error claim is available if one condescends to a consideration of the MacLaurin series expansion for Ln(1 + x):

$$\mathrm{Ln}(1 + x) = x - \frac{1}{2}x^2 + \frac{1}{3}x^3 - \frac{1}{4}x^4 + \cdots . \tag{3-30}$$

For

$$-1 << x << 1, \tag{3-31}$$

(3-30) reduces to the approximate form,

$$\mathrm{Ln}(1 + x) \approx x. \tag{3-32}$$

Now, if

$$x \triangleq 2^{1/N} - 1 \tag{3-33}$$

and N is large enough to validate (3-31), (3-32) yields

$$\mathrm{Ln}(1 + x) = \mathrm{Ln}(2^{1/N}) = \frac{1}{N}\mathrm{Ln}2 \approx 2^{1/N} - 1. \tag{3-34}$$

Combining (3-18) and (3-34),

$$B \approx s_o\left[\frac{\mathrm{Ln}2}{N}\right]^{1/2} = \left(\frac{0.833}{N^{1/2}}\right)s_o, \tag{3-35}$$

which agrees precisely with (3-29). It is thus apparent that (3-28) is an acceptable bandwidth estimation tool for the case of compacted poles. The utility of this tool is enhanced further by the fact that like T_1, T_2 can be discerned directly from the amplifier equivalent circuit, without *a priori* knowledge of pole locations.

The foregoing discloses two distinct bandwidth estimation methods. The first method delivers accurate results if the system poles are widely separated, while the second technique is especially applicable to low-pass structures possessing a dense pole conglomeration. However, at least one serious shortcoming permeates both of these analytical measures: namely, it is impossible to ascertain *a priori* which of the two methods is most acceptable for a given amplifier since rarely, if ever, is explicit information given in regard to amplifier pole conglomeration. In problems where considerable uncertainty in the nature of pole population is justified, the "lumped pole approximation" proves most satisfactory.

The lumped pole method of frequency response estimation is predicated on supplanting the actual circuit transfer function, (3-1), by a transfer relationship having but a single pth-order pole; that is, A(s) in (3-1) is replaced by

$$A_p(s) = \frac{A_o}{(1 + s/s_p)^p} . \tag{3-36}$$

In (3-36), A_o is the true low frequency value of lowpass amplifier gain, while p and s_p are determined in such a way as to make the first two time moments, T_{1p} and T_{2p}, of the lumped model equal respectively to the first two time moments, T_1 and T_2, of the actual system. By modeling the actual N-pole transfer function by one whose parameters are functionally dependent on both T_1 and T_2, the hope intimated by the present theory is the possibility of developing a bandwidth estimate that is insensitive to pole conglomeration.

For (3-36),

$$T_{1p} = \frac{p}{s_p} \tag{3-37}$$

and

$$T_{2p}^2 = \frac{p}{s_p^2} . \tag{3-38}$$

Equating T_{1p} and T_{2p} to T_1 and T_2, respectively, the preceding two expressions are seen to require

$$s_p = \frac{T_1}{T_2^2} \tag{3-39}$$

and

$$p = \left(\frac{T_1}{T_2}\right)^2 . \tag{3-40}$$

Implementation of (3-39) and (3-40) insures that the promulgated lumped pole model possesses first and second time moments that are identical to those of the given lowpass structure. Of particular significance is the fact that since T_1 and T_2 are obtainable directly from the equivalent circuit of the considered system, the computation of s_p and p does not rely on a priori knowledge of critical frequencies.

The expression for bandwidth, say B_p, associated with the lumped pole model is obtainable by setting

$$|A_p(jB_p)| = \frac{|A_o|}{2^{1/2}} . \tag{3-41}$$

It is a trivial matter to show that

$$B_p = s_p(2^{1/p} - 1)^{1/2}, \tag{3-42}$$

or equivalently,

$$B_p = \frac{p}{T_1}(2^{1/p} - 1)^{1/2}. \tag{3-43}$$

Either of the preceding two expressions generate remarkably accurate bandwidth estimates for lowpass structures, independent of the nature of system pole population. In support of this contention, consider the ensuing theoretical discourse.

Reconsider the system defined by (3-1) for the special case of widely separated poles. Then from (3-12), $T_1 \approx T_2$, and by (3-40), $p \approx 1$. Resultantly, (3-43) yields

$$B_p \approx \frac{1}{T_1}(2 - 1)^{1/2} = \frac{1}{T_1},$$

which is identical to the estimated bandwidth delineated in the form of (3-15). If, on the other hand, the system poles are compacted, one may conclude $T_1 \approx N/s_1$ and $T_2^2 \approx N/s_1^2$, whence $p \approx N$. Accordingly, (3-43) renders

$$B_p \approx \frac{N}{T_1}(2^{1/N} - 1)^{1/2} = s_1(2^{1/N} - 1)^{1/2}$$

which is in precise agreement with (3-18), the expression for the bandwidth of a lowpass configuration possessed of an Nth-order pole. It appears that B_p, the lumped pole approximation to lowpass system bandwidth, constitutes an acceptable bandwidth estimate, regardless of the extent of pole separation.

3.1.2 Calculation of First Time Moment

The bandwidth estimation measures developed in the preceding section of material rely heavily on the availability of numerical values for the first and second system time moments. In turn, these moments are functions of critical frequencies which are rarely known explicitly and moreover, they are virtually impossible to obtain conveniently. Accordingly, it is of considerable interest to investigate pragmatic circuit techniques for the enumeration of T_1 and T_2. Actually, only T_1 is considered herewith in deference to two fundamental facts. First, the degree of algebraic complexity associated with computation of T_2 is at least an order of a magnitude larger than the complexities inherent in evaluating T_1. Second, the T_2-method of bandwidth estimation rarely yields results having accuracies that

exceed those produced by the T_1 method since the frequency response of most wideband configurations is inherently more aligned to a dominant pole pattern, rather than a Gaussian pole conglomeration. Thus, T_2 is a useful figure of merit only when it is utilized to generate a lumped pole estimate of circuit bandwidth. Although the accuracy of the latter bandwidth estimation method cannot be denied, the design-oriented utility of lumped pole methodology is unfortunately extremely marginal.

Consider an amplifier having N independently connected capacitors, indicative of existence of an N x 1 state vector. In the interest of analytical expediency, the ensuing discourse is developed in terms of the third order system of figure (3.2), which displays V_1, V_2, V_3 as state variables and I_{1s}, I_{2s}, I_{3s} as independent externally applied forcing functions. Within the linear active network, there can appear only conductances and independent or controlled voltage and current sources. To avoid possible confusion, let it be understood that current sources I_{1s}, I_{2s}, and I_{3s} are included merely in the interest of analytical expediency; they may or may not be present in the given system.

Since there are neither susceptive nor reactive elements within the linear active network diagrammed in figure (3.2), the admittance matrix relating each of the three currents, I_1, I_2 and I_3, to capacitance terminal voltages, V_1, V_2 and V_3, is composed of purely conductive elements. This is to say that

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{21} & g_{22} & g_{23} \\ g_{31} & g_{32} & g_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}, \tag{3-44}$$

where the g_{ij} are real numbers. Inspection of the figure in question shows that

$$I_{js} = I_j + sC_jV_j (j = 1, 2, 3), \tag{3-45}$$

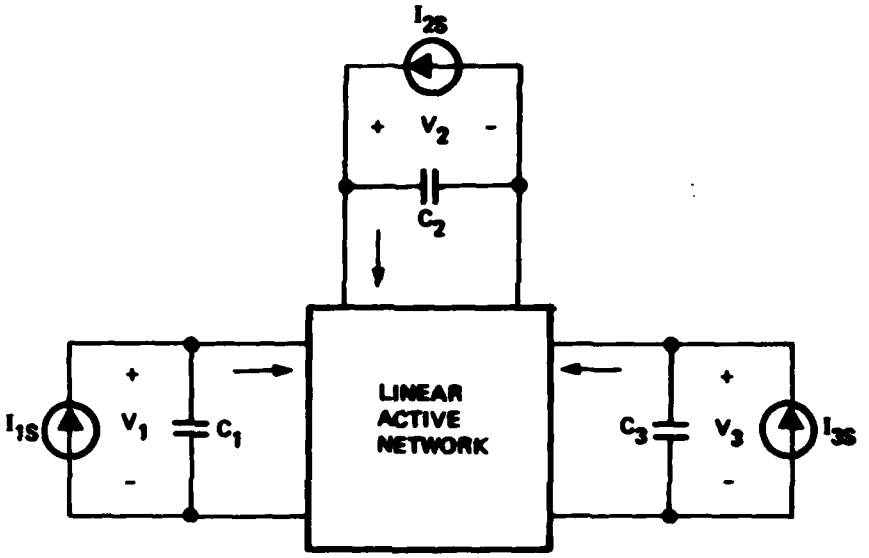


Figure (3.2). A Linear Active System Containing Only Three Storage Elements.

and through use of (3-44), it follows that

$$\begin{bmatrix} I_{1s} \\ I_{2s} \\ I_{3s} \end{bmatrix} = \begin{bmatrix} g_{11} + sC_1 & g_{12} & g_{13} \\ g_{21} & g_{22} + sC_2 & g_{23} \\ g_{31} & g_{32} & g_{33} + sC_3 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}; \qquad (3\text{-}46)$$

in more compact form;

$$\bar{I}_s = \bar{Y}\,\bar{V}. \qquad (3\text{-}47)$$

The $\bar{Y}$-matrix defined by (3-46) and (3-47) is, of course, a short-circuit admittance matrix for the system of figure (3.2). From elementary linear system theory [2], the expression obtained by equating the determinant of $\bar{Y}$, say $\Delta_Y(s)$, to zero comprises the network characteristic equation. Of utmost importance is the observation that if the polynomial in s, $\Delta_Y(s)$, is rendered nomic through term-by-term division by the constant, $\Delta_Y(0)$, the relationship which evolves is the N = 3 version of the denominator appearing on the right-hand side of (3-2):

$$\frac{\Delta_Y(s)}{\Delta_Y(0)} \equiv 1 + b_1 s + b_2 s^2 + b_3 s^3. \qquad (3\text{-}48)$$

Moreover, comparison of the square matrices in (3-44) and (3-46) verifies that $\Delta_Y(0)$, being the s = 0 value of $\Delta_Y(s)$, is identically the determinant, say Δ_g, of the (3 x 3) conductance matrix, $\bar{g}_{ij}$. Thus, (3-48) may be written as

$$\Delta_Y(s) = \Delta_g(1 + b_1 s + b_2 s^2 + b_3 s^3). \qquad (3\text{-}49)$$

The constants b_1, b_2 and b_3 in (3-49) may be expressed in terms of the g_{ij} and C_j through direct expansion of the determinant for the (3 x 3) $\bar{Y}$-matrix appearing in (3-46). For example, the coefficient of

the s^3 term in this expansion is $C_1C_2C_3$ and thus,

$$b_3\Delta_g = C_1C_2C_3. \tag{3-50}$$

Similarly, it turns out that

$$b_2\Delta_g = g_{11}C_2C_3 + g_{22}C_1C_3 + g_{33}C_1C_2 \tag{3-51}$$

and

$$b_1\Delta_g = G_{11}C_1 + G_{22}C_2 + G_{33}C_3, \tag{3-52}$$

where in general, G_{ij} symbolizes the cofactor of g_{ij} in the $\bar{g}$-matrix of (3-44). Utilization of (3-6) leads to the intermediate conclusion,

$$T_1 = \frac{G_{11}}{\Delta_g} C_1 + \frac{G_{22}}{\Delta_g} C_2 + \frac{G_{33}}{\Delta_g} C_3. \tag{3-53}$$

Equation (3-53) relates system first time moment to circuit parameters. Conventional two-port network theory allows straightforward, though admittedly cumbersome, computation of the short-circuit conductance parameters g_{ij}, whereupon numerical values for Δ_g and the G_{ij} follow immediately. Fortunately, the algebraic tedium inherent in this computational approach can be abrogated in favor of an efficient circuits-oriented technique if a number of pertinent observations are exploited. First, note that if C_1, C_2 and C_3 are removed (set equal to zero), from the circuit undergoing study, the $\bar{Y}$-matrix of (3-46) reduces to the $\bar{g}$-matrix of (3-44) and in general, $I_{js} = I_j$ for all cognate j. Then from (3-44),

$$\bar{V} = \bar{g}^{-1}\bar{I}_s = \frac{ADJ(\bar{g})}{\Delta_g} \bar{I}_s, \tag{3-54}$$

where ADJ($\bar{g}$) connotes the adjoint matrix of $\bar{g}_{ij}$. In more explicit terms, (3-54) implies

$$V_j = \sum_{i=1}^{3} \frac{G_{ij} I_{is}}{\Delta_g} \qquad (j = 1, 2, 3). \tag{3-55}$$

It must be remembered that the result in question is applicable for voltage calculation if and only if all capacitors are removed.

In (3-55), the rules of dimensional consistency mandate that G_{ij}/Δ_g be a resistance quantity. In particular, a little thought serves to promulgate the defining argument,

$$\frac{G_{ji}}{\Delta_g} \triangleq r_{ij} \triangleq \frac{V_i}{I_{js}} \Bigg|_{\substack{I_{ks} = 0; \\ k \neq j}} \tag{3-56}$$

that is, resistance r_{ij} is the ratio of ith voltage to jth current in figure (3.2), under the condition that all currents except the jth be set equal to zero. As such, r_{ij} is an open circuit ("open," meaning all capacitors are removed) resistance entity realized when all independent sources of energy are made to vanish. The stipulation of all, as opposed to merely the I_{ks}, independent sources removed is very much in concert with the Thevenin definition of resistance.

The consideration of the special case, i = j, is particularly interesting since $r_{jj} = G_{jj}/\Delta_g$ boasts a form identical to the capacitor coefficients appearing on the right-hand side of (3-53). Moreover,

$$r_{jj} = \frac{G_{jj}}{\Delta_g} = \frac{V_j}{I_{js}} \Bigg|_{\substack{I_{ks} = 0 \\ k \neq j}} \tag{3-57}$$

represents the zero-capacitance value of resistance seen looking into the terminal pair across which C_j is to be connected. It is therefore meaningful to rewrite (3-53) as

$$T_1 = \sum_{j=1}^{3} \tau_{jj}, \tag{3-58}$$

where

$$\tau_{jj} = r_{jj}C_j \tag{3-59}$$

is the open circuit (in the sense that all capacitors are open-circuited) time constant associated with capacitor C_j.

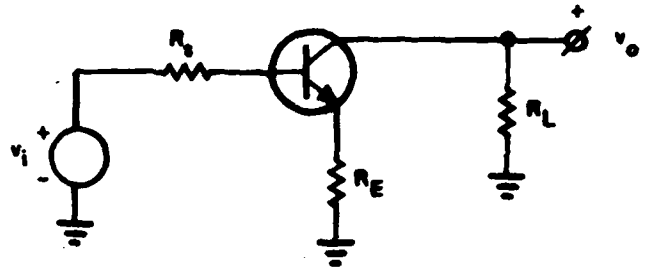
It is intuitively clear that for an Nth order system, N terms are summed on the right-hand side of (3-58). Accordingly and because of (3-15),

$$B_w = \frac{1}{\sum_{j=1}^{N} \tau_{jj}}. \tag{3-60}$$

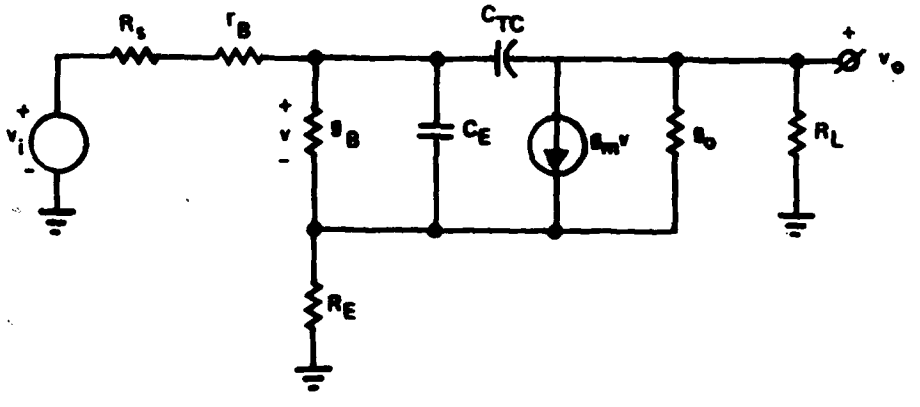
Equation (3-60) is the mathematical definition of the so-called "open circuit time constant method" of bandwidth estimation.

3.1.3 Common Emitter/Common Base Cascode

An excellent demonstration of the utility of (3-60) is afforded by investigating the bandwidth enhancement which accures when a common base cascode stage is utilized to couple a resistive load to a simple feedback amplifier. To this end, consider a simple current feedback configuration whose AC schematic diagram is displayed in figure (3.3a). Figure (3.3b) offers the small-signal hybrid-pi model, wherein all parameters have their usual interpretations [3].



(a)



(b)

Figure (3.3). (a) AC Schematic Diagram of Simple Current Feedback Amplifier.

(b) Small-Signal Hybrid-Pi Model.

It is easily shown that the low frequency voltage gain is

$$A_o = \left.\frac{V_o(j\omega)}{V_i(j\omega)}\right|_{\omega = 0} = \frac{h'_{fe}R_L}{\frac{1}{g_B} + R_s + r_B + (h'_{fe} + 1)R_E}, \qquad (3\text{-}61)$$

where

$$h'_{fe} = \frac{g_m/g_B - g_oR_E}{1 + g_o(R_L + R_E)}. \qquad (3\text{-}62)$$

Assuming a dominant pole response, the frequency response derives from

$$A(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} \approx \frac{A_o}{1 + j\omega T_1} \qquad (3\text{-}63)$$

with T_1 representing the circuit first time moment. Equation (3-63) is valid through the neighborhood of the 3-dB bandwidth, B, given approximately by

$$B \approx B_w = \frac{1}{2\pi T_1} \text{ (hz)}. \qquad (3\text{-}64)$$

Parameter T_1 is the sum of the open circuit time constants attributed respectively to C_E and C_{TC}. Figure (3.4a) is the circuit pertinent to computing the open circuit time constant due to C_E, while figure (3.4b) is the circuit for C_{TC} calculations. Thus,

$$T_1 = r_{11}C_E + r_{22}C_{TC} \qquad (3\text{-}65)$$

where, from figure (3.4a),

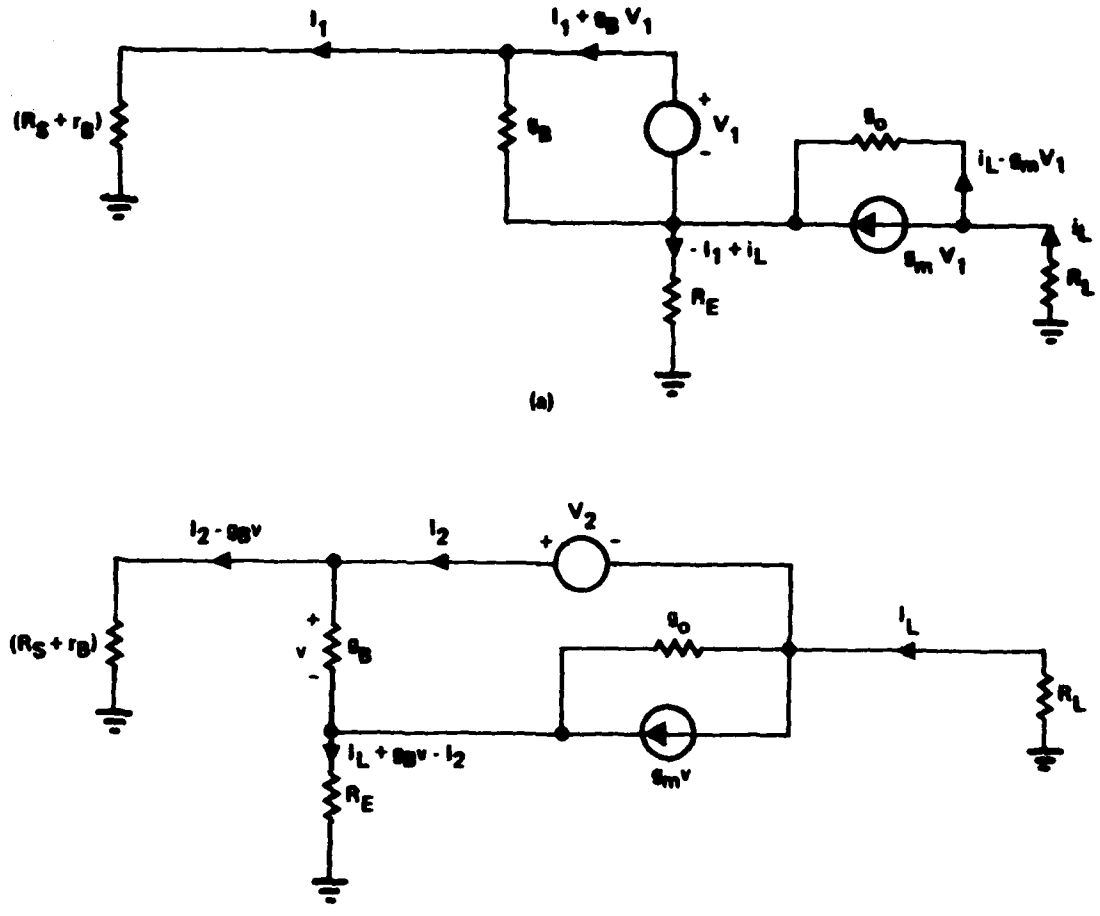


Figure (3.4). (a) Circuit for Evaluating r_{11} in (3-65).

(b) Circuit for Evaluating r_{22} in (3-65).

$$r_{11} = \frac{1}{g_B} \| \frac{V_1}{I_1} = \frac{1}{g_B} \| \left\{ \frac{R_s + r_B + R_E \| (R_L + 1/g_o)}{1 + \frac{g_m R_E}{1 + g_o(R_L + R_E)}} \right\}. \tag{3-66}$$

while by figure (3.4b),

$$r_{22} = \frac{V_2}{I_2} = (R_s + r_B) \left\{ \frac{1 + g_B R_E \left[(h'_{fe} + 1) - \frac{g_o R_L}{1 + g_o(R_L + R_E)} \right]}{1 + g_B [R_s + r_B + (h'_{fe} + 1) R_E]} \right\}$$

$$+ R_L \left\{ \frac{1 + g_o R_E}{1 + g_o(R_L + R_E)} + \frac{h'_{fe} \left[(R_s + r_B) + \frac{g_o R_E / g_B}{1 + g_o(R_L + R_E)} \right]}{\frac{1}{g_B} + R_s + r_B + (h'_{fe} + 1) R_E} \right\}. \tag{3-67}$$

If g_o is small,

$$h'_{fe} \approx g_m / g_B = h_{fe}, \tag{3-68}$$

$$r_{11} \approx \frac{R_s + r_B + R_E}{1 + g_B(R_s + r_B) + (g_m + g_B) R_E}, \tag{3-69}$$

$$r_{22} \approx \frac{(R_s + r_B)[1 + (g_m + g_B) R_E]}{1 + g_B(R_s + r_B) + (g_m + g_B) R_E}$$

$$+ R_L \left\{ \frac{1 + (g_m + g_B)(R_s + r_B + R_E)}{1 + g_B(R_s + r_B) + (g_m + g_B) R_E} \right\}. \tag{3-70}$$

Because of (3-65), it is clear that large R_L, hence large gain, is detrimental to bandwidth, owing to the direct dependence of r_{22} on a multiplicative factor of R_L. Note further that the effect of R_E is

to increase bandwidth, at the expense of gain, through reduction of r_{11}.

By interposing a common base stage between the load and the emitter degenerated first stage of amplification, the last term in (3-70) is significantly reduced since in effect, R_L becomes the inherently low input resistance of a common base amplifier. The situation is depicted in figure (3.5a), with the equivalent circuit offered as figure (3.5b). Note that g_o is ignored, as per (3-68) through (3-70). To be sure, additional terms are now added to the first time moment, as calculated below.

The low frequency voltage gain of the network in question can be shown to be

$$A_{OB} = \left.\frac{V_o(j\omega)}{V_i(j\omega)}\right|_{\omega=0} = -\left(\frac{h_{fe}}{h_{fe}+1}\right)\left\{\frac{h_{fe}R_L}{\frac{1}{g_B}+R_s+r_B+(h_{fe}+1)R_E}\right\}, \tag{3-71}$$

where in general,

$$A_B(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} \approx \frac{A_{OB}}{1+j\omega T_{1B}}. \tag{3-72}$$

In (3-72), T_{1B} is the first time moment produced by the four network capacitors apparent in figure (3.5b). In particular,

$$\begin{aligned} T_{1B} &= r_{11B}C_{E1} + r_{22B}C_{TC1} + r_{33B}C_{E2} + r_{44B}C_{TC2} \\ &= (r_{11B}+r_{33B})C_E + (r_{22B}+r_{44B})C_{TC}, \end{aligned} \tag{3-73}$$

assuming that each device is biased similarly to produce nominally equivalent corresponding capacitor values. In (3-71),

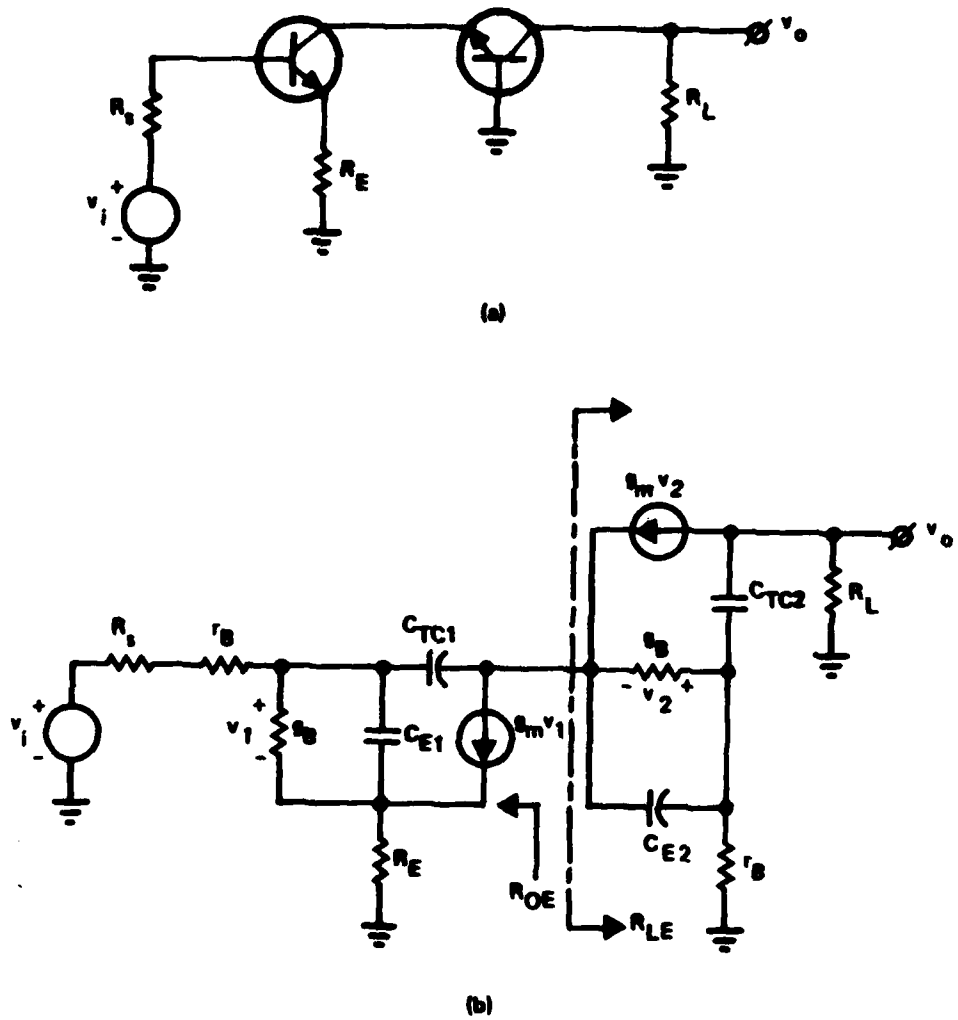


Figure (3.5). (a) Common Emitter-Common Base Cascode With Current Feedback in First Stage.

(b) Simplified Small-Signal Model.

$$h_{fe} = g_m/g_B, \tag{3-74}$$

which is identical to h'_{fe} in (3-62) with the proviso that $g_o = 0$. Moreover, observe that to the extent that $h_{fe} >> 1$, A_{OB} in (3-71) and A_o in (3-61) are virtually identical.

It can be shown that the open circuit resistance facing capacitor C_{E1} is

$$r_{11B} \equiv r_{11}, \tag{3-75}$$

as defined by (3-69), while the open circuit resistance facing capacitor C_{TC1} is

$$r_{22B} = \frac{(R_s + r_B)[1 + (g_m+g_B)R_E]}{1 + g_B(R_s + r_B) + (g_m + g_B)R_E}$$

$$+ R_{LE}\left\{\frac{1 + (g_m + g_B)(R_s + r_B + R_E)}{1 + g_B(R_s + r_B) + (g_m + g_B)R_E}\right\}. \tag{3-76}$$

In (3-76), R_{LE} represents the net DC input resistance of the common base stage and is given by

$$R_{LE} = \frac{1 + g_B r_B}{g_m + g_B}. \tag{3-77}$$

Note that if R_L in (3-70) is supplanted by R_{LE}, r_{22} and r_{22B} are identical.

Since the output resistance, R_{OE}, of the current feedback unit is infinitely large at low frequencies, the open circuit resistance facing C_{E2} is

$$r_{33B} = \frac{1}{g_m + g_B} . \tag{3-78}$$

Similarly, r_{44B}, the resistance parameter pertinent to C_{TC2}, is

$$r_{44B} = R_L + r_B. \tag{3-79}$$

Equations (3-75), (3-76), (3-78), and (3-79) may now be inserted into (3-73) to ascertain the first time moment, and resultantly the estimated bandwidth of the cascode configuration. It is illuminating to accomplish this algebraic manipulation in a manner which unambiguously compares the cascoded time moment to the time moment of the original, uncompensated circuit of figure (3.3a). If $(g_m + g_B)$ is taken to be large and, of course, if g_o is presumed to be negligibly small, one can show that

$$T_{1B} \approx T_1 + \left\{ r_B - \frac{R_L}{R_E} (R_s + r_B) \right\} C_{TC}, \tag{3-80}$$

where T_1 is the first time moment of the uncompensated configuration. This result clearly demonstrates that the cascoded bandwidth, which is inversely proportional to T_{1B}, is larger than the original bandwidth, which is inversely related to T_1, provided

$$\frac{R_L}{R_E} > \frac{r_B}{r_B + R_s} . \tag{3-81}$$

Since R_L/R_E is approximately the magnitude of voltage gain in the original circuit, especially if g_m itself is large, it seems reasonable to suspect straightforward satisfaction of (3-81).

3.1.4 Model Reduction

In addition to expediting design-oriented calculations at the circuit level, time moment theory can also be used to reduce complicated small-signal device models to topologies that allow for tractable manual analyses. The small-signal equivalent circuit for OAT devices is indeed analytically troublesome, owing to the apparent need to model base region dynamics by a two-lump RC section. However, methodical application of the first time moment concept allows for straightforward reduction of an OAT model to the traditional, and more manageable, hybrid-pi structure.

The small-signal model pertinent to the analysis and design of OAT RF circuits is given in figure (3.6). Intrinsic base resistance r_{B2}, base-emitter junction diffusion resistance R_{pi}, base-emitter junction diffusion capacitance C_{pi}, collector-base junction depletion capacitance C_{μ}, forward transconductance g_m, and output Early resistance R_o are automatically incorporated by SPICE-2 program architecture during the course of a linearized small-signal computer-aided analysis [4]. Likewise, series emitter resistance r_e, collector resistance r_{C1}, and a voltage-invariant substrate capacitance, C_{cs}, are also included in conventional SPICE-2 small-signal topology. Branch element parameters C_{BC}, r_{B1}, r_{C2}, and a voltage-variant substrate capacitance evolve in a SPICE-2 circuit simulation only if the appropriate OAT macromodel [5] is utilized. Needless to say, the substrate terminal is in electrical contact with the circuit node across which the most negative circuit potential is sustained.

Two fundamental analytical problems prevail with the considered circuit model. First, the model is sufficiently complicated to preclude a reasonably accurate and efficient manual analysis of anticipated device performance in a given circuit application. Manual circuit investigations are more readily accomplished if one can assume that C_{BC}, C_{cs}, r_{C1}, r_{C2}, and r_e are all equal to zero which, in effect, collapses the indicated model to the simple hybrid-pi structure found in the elementary electronics literature. Unfortunately, such a

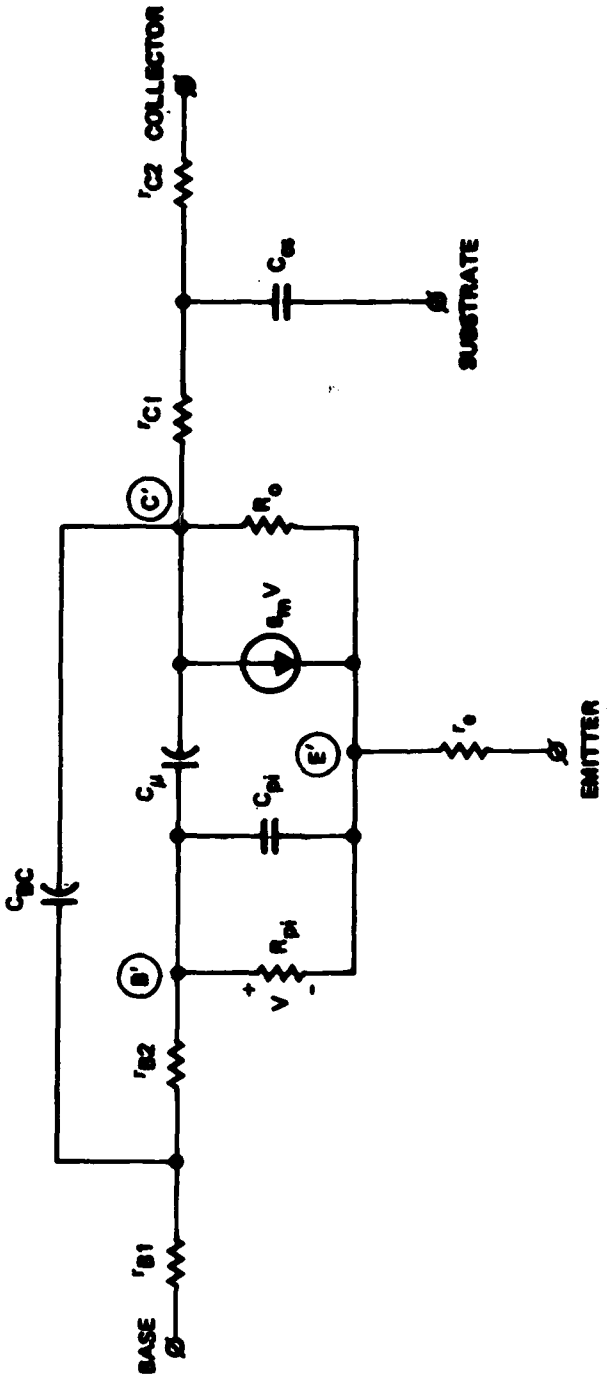


Figure (3.6). OAT Small-Signal Model.

simplified analytical tact precipitates unacceptably optimistic performance estimates.

A second problem arises from the fact that the appended branch element parameters, r_{B1}, C_{BC} and r_{C2}, in the OAT macromodel obscure the mathematical definition of transistor gain-bandwidth product, f_T, and small-signal low frequency current gain, β_o. Indeed, SPICE-2 inherently ignores the effects that appended macromodel elements exert on both f_T and β_o. There is even some doubt that the numerical values of f_T and β_o printed as outputs in a small-signal SPICE-2 exercise properly incorporate the performance degradations incurred by presumably second order dynamical effects in the base, collector, and base-collector overlap branch. The upshot of the matter is that a parameter determination procedure founded in part on matching printed values of f_T and β_o to measured values of these respective parameters can lead to unrealistic model parameters.

The first step in the model reduction process is to absorb r_e into the topology embedded among nodes B', C', and E'. It can be shown that with

$$F_E \triangleq 1 + \left(g_m + \frac{1}{R_{pi} \| R_o}\right) r_e \tag{3-82}$$

and for radial signal frequencies which conform to the constraint,

$$\omega << \frac{F_E}{r_e C_{pi}}, \tag{3-83}$$

the model offered in figure (3.7) is a valid representation of small-signal transistor performance. Resistive source and load terminations, R_S and R_L, are introduced for subsequent convenience, and it is assumed that the emitter lies at the lowest circuit potential. If the latter assumption is not valid, the substrate capacitance branch must be

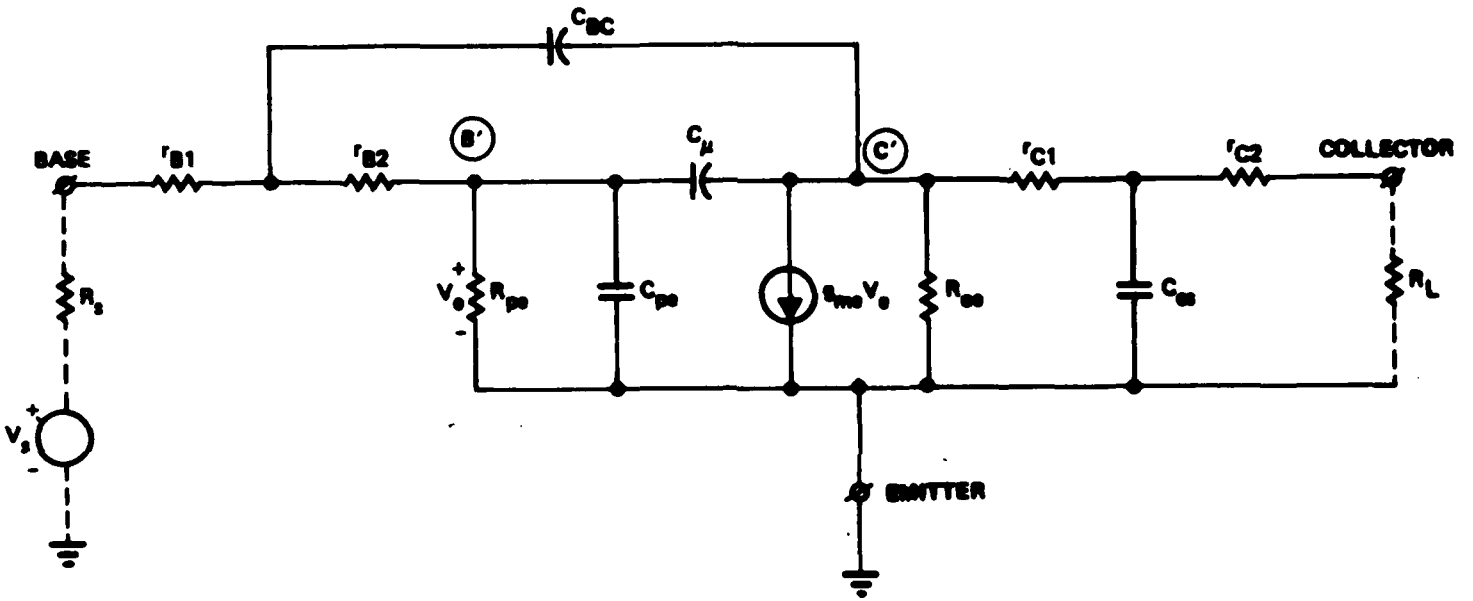


Figure (3.7). Approximate Hybrid-Pi OAT Model With Emitter Resistance r_e Absorbed Into Instrinsic Pi Structure.

connected between the junction of r_{C1}-r_{C2} and the appropriate node. Furthermore,

$$\left.\begin{aligned} R_{pe} &= F_E R_{pi} \\ R_{oe} &= F_E R_o \\ C_{pe} &= C_{pi}/F_E \\ g_{me} &= g_m/F_E \end{aligned}\right\}. \tag{3-84}$$

It must be understood that R_{pi}, R_o, C_{pi} and g_m are SPICE-2 printouts, while R_{pe}, R_{oe}, C_{pe} and g_{me} are artifacts which allow for convenient consideration of series emitter resistance r_e. Moreover, C_{pi} includes both transition and diffusion components of net base-emitter junction capacitance. Finally, observe that the effective pi parameters reduce to their counterpart SPICE-2 printouts in the limit as r_e approaches zero.

The order of complexity of the resultant network model is obviously four. The four pole frequencies are likely to be real for resistive source and load terminations, and the magnitude of the zeros produced by C_{BC} and C_μ are invariably large in comparison to the dominant poles. The latter assertion derives from the reasonable presumption that forward signal transmission is far more significant than reverse signal transport from collector-to-base. Within the context of the foregoing stipulations and the additional assumption that the circuit exudes a dominant pole response, the 3-dB bandwidth is

$$B_{3dB} \approx \frac{1}{2\pi \sum_{j=1}^{4} \tau_{jo}}, \tag{3-85}$$

where τ_{jo} is the time constant associated with capacitor C_j under the condition that all other capacitors are open-circuited.

In figure (3.7),

$$\frac{1}{2\pi B_{3dB}} \approx r_{pe}C_{pe} + r_{\mu}C_{\mu} + r_{BC}C_{BC} + r_{cs}C_{cs}, \tag{3-86}$$

where r_{pe} is the resistance facing C_{pe} with C_{μ}, C_{BC}, and C_{cs} open-circuited. The other resistance parameters in (3-86) are analogously defined. Equation (3-86) can be rewritten as

$$\frac{1}{2\pi B_{3dB}} \approx r_{pe}C_{pe} + r_{\mu}C_{m}(R_s,R_L) \tag{3-87}$$

with

$$C_m(R_s,R_L) = C_{\mu} + \left(\frac{r_{BC}}{r_{\mu}}\right)C_{BC} + \left(\frac{r_{cs}}{r_{\mu}}\right)C_{cs} \tag{3-88}$$

denoting an effective junction capacitance that is functionally dependent on source and load resistances. These two results suggest that insofar as the estimation of feed-forward response characteristics is concerned, the model depicted in figure (3.8) is precisely identical to that of figure (3.7). It is to be emphasized that the two models are identical only in the sense that both predict identical low frequency gains and resistances and additionally, both networks predict the same approximate 3-dB bandwidth of the forward gain characteristic.

Letting

$$R_s' \triangleq \frac{R_{pe}(R_s + r_{B1})}{R_{pe} + R_s + r_{B1} + r_{B2}} \tag{3-89}$$

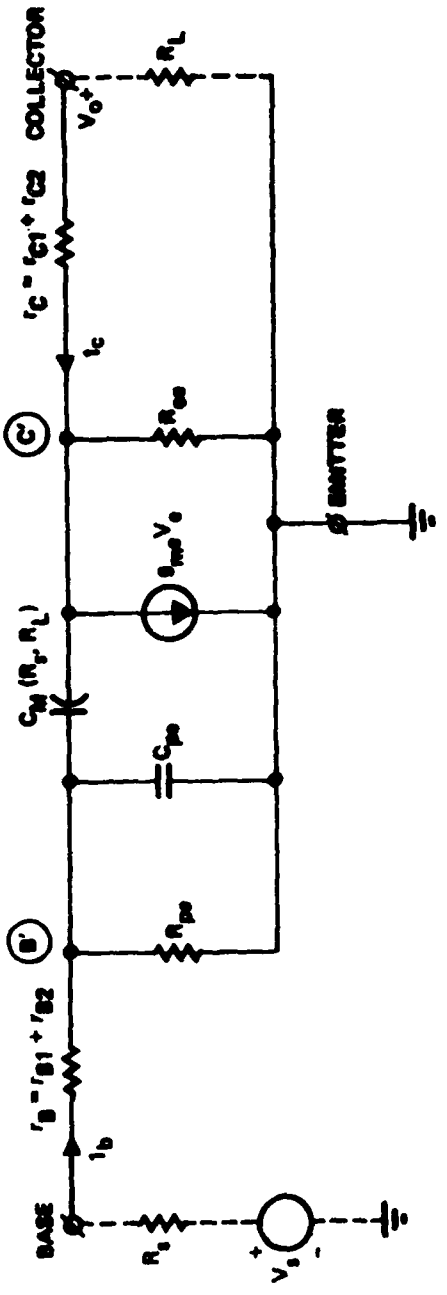


Figure (3.8). Simplified 2-Pole Model Which Predicts the Same Low Frequency Characteristics and Forward 3-dB Bandwidth Estimate as Does the Model of Figure (3.7).

and

$$R_L' = R_{oe} \ (r_{C1} + r_{C2} + R_L), \tag{3-90}$$

it can be shown that

$$\frac{r_{BC}}{r_\mu} = \frac{R_L' + (1 + g_{me}R_L' + r_{B2}/R_{pe})R_s'}{R_L' + (1 + g_{me}R_L')r_{pe}}, \tag{3-91}$$

$$r_{pe} = R_{pe} \| (r_{B1} + r_{B2} + R_s), \tag{3-92}$$

and finally,

$$\frac{r_{cs}}{r_\mu} = \frac{(r_{C1} + R_{oe}) \| (r_{C2} + R_L)}{R_L' + (1 + g_{me}R_L')r_{pe}}. \tag{3-93}$$

Note that for $r_{B2} << R_{pe}$ and $r_{B2} << R_s$, $R_s' \approx r_{pe}$ and r_{BC}/r_μ reduces to unity, as expected. Moreover, note that the contribution to bandwidth deterioration due to substrate capacity is negligible since for large effective transconductance, r_{cs}/r_μ in (3-93) is small.

The advantage of the model displayed in figure (3.8) is that it enables the computation of voltage gain and current gain by inspection. Moreover, the classical expressions for device gain-bandwidth product and device unity power gain frequency can be utilized directly, provided that the time constants associated with C_{pe} and $C_M(R_s,R_L)$ are judiciously calculated.

For example, the low frequency voltage gain, A_{VO}, of the circuit in figure (3.8) is

$$A_{VO} = \left(\frac{V_o}{V_s}\right) = \left(\frac{V_o}{V_e}\right)\left(\frac{V_e}{V_s}\right)$$

$$= -(g_{me}R_L)\left(\frac{R_{oe}}{R_{oe} + r_c + R_L}\right)\left(\frac{R_{pe}}{R_{pe} + r_B + R_s}\right)$$

and using (3-84),

$$A_{VO} = -(g_m R_{pi})\left(\frac{F_E R_o}{F_E R_o + r_c + R_L}\right)\left(\frac{R_L}{F_E R_{pi} + r_B + R_s}\right). \qquad (3\text{-}94)$$

Likewise, the low frequency current gain, A_{IO}, is

$$A_{IO} = \frac{i_c}{V_s/R_s} = \left(\frac{i_c}{V_e}\right)\left(\frac{V_e}{V_s}\right)R_s$$

$$= \frac{g_m R_{pi}}{\left(1 + \dfrac{r_B + F_E R_{pi}}{R_s}\right)\left(1 + \dfrac{r_c \quad R_L}{F_E R_o}\right)}. \qquad (3\text{-}95)$$

For the case of $R_s \to \infty$ and $R_L = 0$, A_{IO} becomes the short circuit common emitter current gain,

$$h_{feo} = \frac{g_m R_{pi}}{1 + r_c/F_E R_o}. \qquad (3\text{-}96)$$

The gain-bandwidth product figure of merit, f_T, is expressible as

$$f_T = \frac{g_{me}}{2\pi[C_{pe} + C_m(\infty,0)]} = \frac{g_m}{2\pi[C_{pi} + F_E C_m(\infty,0)]} \qquad (3\text{-}97)$$

where $C_m(\infty,0)$ is the value of $C_m(R_s,R_L)$ pertinent to a current source signal drive and short circuited load. Thus, in (3-89) through (3-93), the values of R_s' and R_L' used in calculating $C_m(\infty,0)$ are

$$R_s' = r_{pe} = R_{pe} = F_E R_{pi} \tag{3-98}$$

and

$$R_L' = R_{oe}\, r_c = F_E R_o\, r_c. \tag{3-99}$$

The power gain that a bipolar transistor is capable of supplying is within 3-dB of the true maximum power gain when the load is conjugately matched to the short circuit output admittance, Y_{oe}, of the device [6]. It is, of course, tacitly assumed that the transistor is unconditionally stable for such a load condition. Using the model of figure (3.8), it can be shown that the frequency f_{MAX}, where the indicated power gain degrades to unity, is

$$f_{MAX} = \frac{1}{2\pi}\left\{\frac{g_m}{4r_B(C_{pi} + F_E C'_m)C'_m}\right\}^{1/2} \tag{3-100}$$

where C'_m is the value of C_m computed under the conditions, $R_s = 0$ and $1/R_L = R_e(Y_{oe})$. A crude, but nominally adequate approximation of $R_e(Y_{oe})$ at high frequencies is

$$R_e(Y_{oe}) = \frac{1}{r_{c'}} \tag{3-101}$$

and accordingly in (3-100),

$$C'_m = C_m(0,r_c). \tag{3-102}$$

In order to exemplify the foregoing theory, consider a three-stage differential amplifier, for which the SPICE-2 small-signal parameters at a collector current of 2 MA and a collector-emitter voltage of 4.9 volts are outputted as

g_m = 69.2 mmhos,

R_{pi} = 872 ohms,

R_o = 9.53 K-ohms,

C_{pi} = 2.08 pF (includes transition component),

C_μ = 0.0173 pF.

Additionally,

r_e = 1 ohm,

r_{C1} = 60 ohms,

r_{C2} = 34 ohms,

r_{B1} = 16 ohms,

r_{B2} = 80 ohms,

C_{BC} = 0.38 pF,

C_{cs} = 0.4 pF.

The gain-bandwidth product, f_T, is to be computed and accordingly, $R_S = \infty$ and $R_L = 0$.

From (3-82) and (3-84),

F_E = 1.070,

R_{pe} = 933 ohms,

R_{oe} = 10.201 K-ohms,

C_{pe} = 1.943 pF,

g_{me} = 64.646 mmhos.

Using (3-96),

$$h_{feo} = 59.791,$$

which compares favorably with the SPICE-2 printout of 60.345. With $R_S = \infty$ and $R_L = 0$, (3-89) through (3-93) deliver

$$R_S' = R_{pe} = 933 \text{ ohms},$$

$$R_L' = 93.142 \text{ ohms},$$

$$r_{pe} = R_{pe} = 933 \text{ ohms},$$

$$\frac{r_{BC}}{r_\mu} = 1.012,$$

$$\frac{r_{cs}}{r_\mu} = (5.098)(10^{-3}).$$

Then by (3-88) and (3-97),

$$C_m(\infty,0) = 0.404 \text{ pF}$$

and

$$f_T = 4.38 \text{ GHz}.$$

The SPICE-2 printout, which does not consider the macro elements, is $f_T = 5.70$ GHz.

In order to compute f_{MAX}, one sets $R_S = 0$ and $R_L = r_c = 94$ ohms. Then

$$R_S' = 14{,}508 \text{ ohms},$$

$$R_L' = 184.60 \text{ ohms},$$

$$r_{pe} = 87.048 \text{ ohms},$$

$$\frac{r_{BC}}{r_\mu} = (285.01)(10^{-3}),$$

$$\frac{r_{cs}}{r_{\mu}} = (96.475)(10^{-3}),$$

and

$$C_m(0,r_c) = 0.1642 \text{ pF} = C'_m.$$

From (3-100),

$$f_{MAX} = 3.51 \text{ GHz},$$

which is presumably the highest frequency at which greater than unity power gain is achievable for the stipulated bias conditions.

3.2 Two-Port Power Flow Model

It is difficult to debate the assertion that the most satisfying electronic circuit design methodology is one which revolves around active device models whose topology and parameters derive directly from monolithic fabrication characteristics and the fundamental physics underlying device performance. Unfortunately, the state of the modeling art has not yet matured to a level that allows formulation of an explicit and general relationship between circuit performance and process characteristics. Additionally, the physics of transistor action implicit in OAT technology is sufficiently complicated to preclude delineation of a satisfying physical model that is useful over a broad variety of operational environments.

In deference to the foregoing situation, the transistor models used in the circuit design cycle of RFLSI are largely predicated on measured electrical terminal characteristics. In particular, the scattering parameters are generally measured at numerous frequencies for a variety of bias conditions. It is possible to convert these scattering parameters into conventional two port parameters, such as the short circuit admittance parameters, and from this converted parameter set, a useful small signal circuit model of the device presumably

evolves. If the highest frequency at which scattering parameters are measured is nominally ten percent of the device short circuit gain bandwidth product, f_T, the model in question can be cast in the topological form of figure (3.6). This state of affairs is very much desirable since the branch elements of this model bear an explicit dependence on transistor large signal parameters, which in turn are at least implicitly related to process characteristics and physical considerations.

At higher frequencies, the distributed dynamics associated with active base and collector regions of OAT devices preclude a hybrid pi representation of small-signal transistor behavior. The alternative is a traditional two port equivalent circuit, as shown in figure (3.9). The Y_{ij} in this model are extracted from measured scattering parameters, while Y_S and Y_L respectively denote general source and load terminations at transistor input and output ports. Despite the fact that the Y_{ij} are nonphysical entities that are sensitive to both bias and signal frequency perturbations, the model is useful in both IF and RF design applications.

3.2.1 Power Flow Representation

Because the model in figure (3.9) is linear, it is permissible to take advantage of the computational simplifications that accrue from the normalization,

$$V_1 \triangleq 1 + j0. \tag{3-103}$$

From figure (3.9), voltage V_2 is seen as being proportional to Y_{21} and inversely dependent on the admittance function, $(Y_{22} + Y_L)$. Since Y_{21}, Y_{22}, and Y_L are in general complex admittances, V_2 is likely to be a complex voltage. It is convenient to express the invariably complex nature of V_2 in the form,

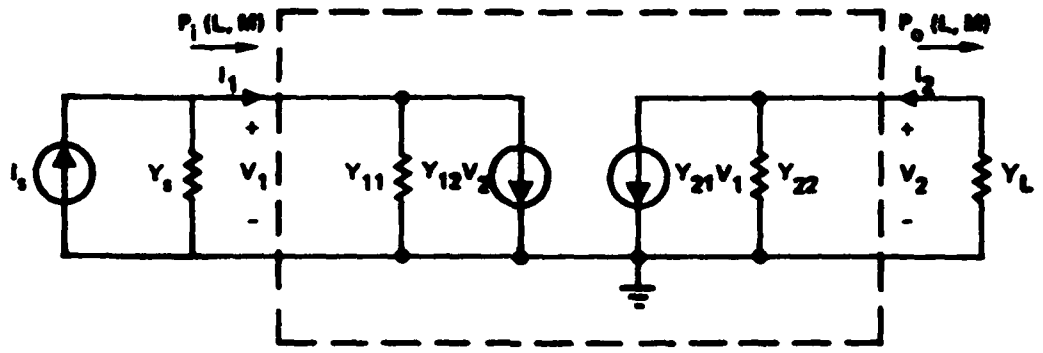


Figure (3.9). Two-Port Model of OAT Transistor.

$$V_2 \triangleq \frac{-Y_{21}}{2\mathrm{Re}(Y_{22})} (L + jM). \tag{3-104}$$

Observe that this definition is structured such that (L,M) = (1,0) is placed in one-to-one correspondence with a load conjugately matched to short-circuit output admittance, Y_{22}. This assertion derives from the fact that with $V_1 = 1$, $V_2 = -Y_{21}/2\mathrm{Re}(Y_{22})$ if and only if $Y_L = Y^*_{22}$.

An inspection of figure (3.9) shows that the input admittance is given by

$$Y_{in}(j\omega) = \frac{I_1}{V_1} = I_1 = Y_{11} - \frac{Y_{12}Y_{21}}{2\mathrm{Re}(Y_{22})} (L + jM) \tag{3-105}$$

or

$$Y_{in}(j\omega) = \left[g_{11} - \left(\frac{aL - bM}{2g_{22}}\right)\right] + j\left[b_{11} - \frac{bL + aM}{2g_{22}}\right]. \tag{3-106}$$

In (3-106),

$$Y_{12}Y_{21} \triangleq a + jb \tag{3-107}$$

$$Y_{11} \triangleq g_{11} + jb_{11} \tag{3-108}$$

$$Y_{22} \triangleq g_{22} + jb_{22}. \tag{3-109}$$

It follows that the power delivered to the network input port is

$$P_i(L,M) = |V_1|^2 \mathrm{Re}[Y_{in}(j\omega)] = g_{11} - \frac{aL - bM}{2g_{22}}. \tag{3-110}$$

A number of noteworthy points can now be brought to light. First, when plotted in the L-M plane, $P_i(L,M)$ is itself a plane whose gradient is largely determined by the admittance product, $Y_{12}Y_{21}$. This is to say that the inclination of the $P_i(L,M)$ surface with respect to the M-axis is directly proportional to $I_m(Y_{12}Y_{21})$, while the slope of $P_i(L,M)$ with respect to L is directly related to $Re(Y_{12}Y_{21})$. Thus, in a so-called unilateralized amplifier, which has $Y_{12} = 0$, the $P_i(L,M)$ plane is parallel to the L-M plane, and as verified by (3-110), the unilateralized $P_i(L,M)$ surface is elevated above the L-M plane by an amount equal to $Re(Y_{11})$. Figure (3.10) portrays the general nature of input power as a function of L and M.

For $Y_{12} \neq 0$, the foregoing discussion suggests the existence of values of L and M for which $P_i(L,M)$, and hence, $Re[Y_{in}(j\omega)]$, is negative. From (3-110), $P_i(L,M) \geq 0$ if

$$M \geq \left(\frac{a}{b}\right)L - \frac{2g_{11}g_{22}}{b} ; \qquad (3\text{-}111)$$

the locus defined by the right-hand side of this equation is plotted in figure (3.11). Points on the locus correspond to zero input power, values of M lying above the straight line give rise to positive input power, and points below the locus produce negative input power; that is, the input port of the network delivers power to the source termination.

Since negative input power requires negative input conductance by virtue of (3-110) and (3-106), it may appear logical to presume that the dissatisfaction of (3-111) is an undesirable state of affairs. Unfortunately, this reasoning is somewhat premature unless one is assured that the values of M and L which do not satisfy (3-111) correspond to a passive load termination. If the values of M and L that are of present concern indeed define a passive load admittance Y_L, the direction of output power flow is as shown in figure (3.9); that is, Y_L consumes power and cannot generate power for delivery to the output port of the network. In such an event, a negative input conductance, which gives

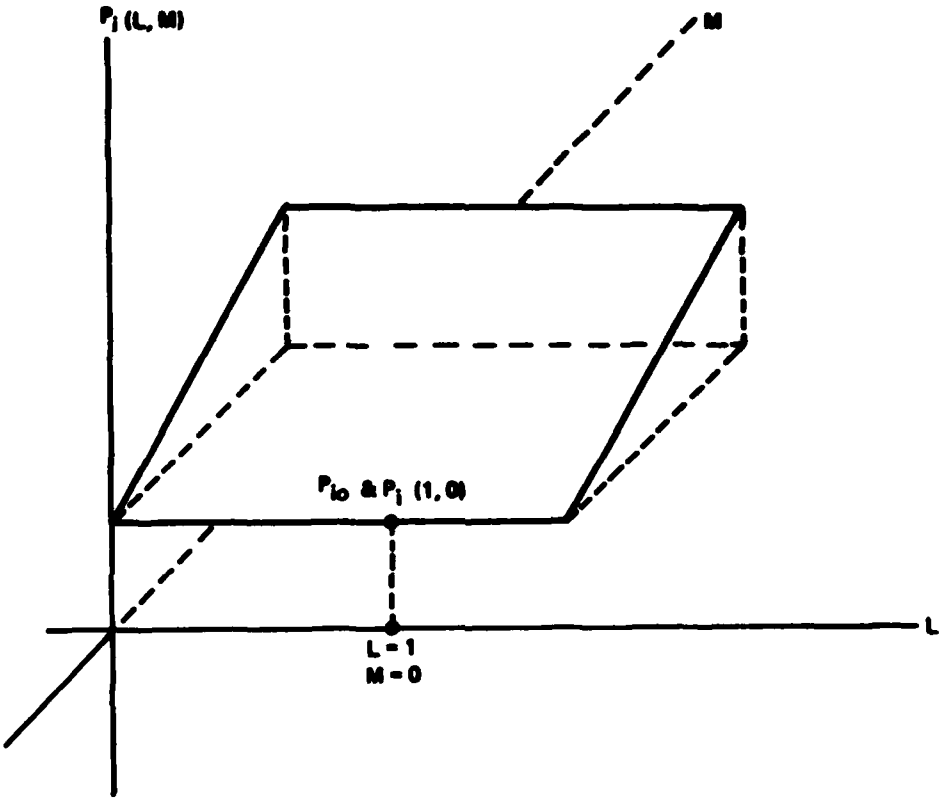


Figure (3.10). Power Input as a Function of (L,M).

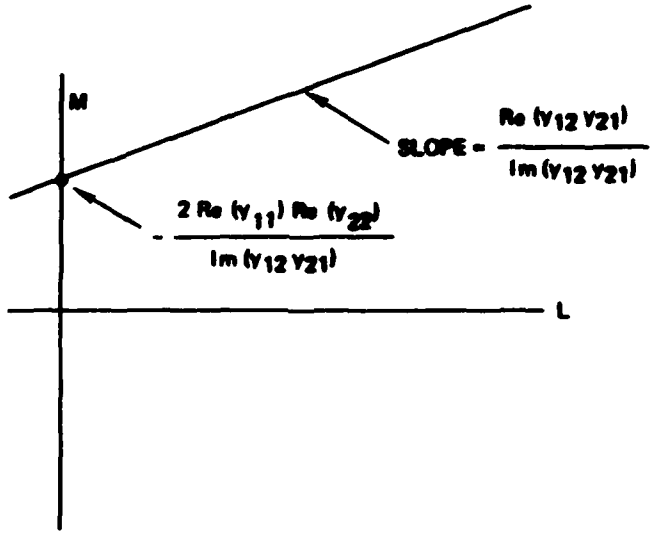


Figure (3.11). Locus of Zero Input Power in the L-M Plane. Locus is shown for the special case of negative real and imaginary parts of $(Y_{12}Y_{21})$.

rise to a flow of input power that is opposite to the direction depicted in figure (3.9), must imply network oscillation or instability, since one is lead to the incongruent conclusion that the presumably linear and relaxed two-port network is a source of energy at either of its ports. Stated in more direct terms, if the real part of the input admittance is negative for a fixed passive load at a given frequency, say ω_o, there exists a passive source admittance Y_S, such that $Y_S(j\omega_o) + Y_{in}(j\omega_o) = 0$, thereby rendering

$$V_1(\omega_o) = \frac{I_S}{Y_S(j\omega_o) + Y_{in}(j\omega_o)} \tag{3-112}$$

independent of source excitation I_S. Clearly, this situation does not corroborate with presumed network linearity, and one is therefore forced to conclude that the network is oscillatory or self-sustaining at radial frequency ω_o. On the other hand, if the M and L that do not satisfy (3-111) define an active load, power flows to the output port from the load. Resultantly, the flow of power from the input port to the source termination does not necessarily correspond to network instability for in effect, the two-port is merely transmitting power in the reverse direction. Therefore, (3-111) is a meaningful stability criterion if and only if the values of M and L to which attention is addressed is commensurate with a passive load termination.

Returning to (3-106), it can be seen that the normalizations postulated in (3-103) and (3-104) permit the definition of load terminations conducive to a purely real, capacitive, or inductive input admittance. For example,

$$M = \frac{2g_{22}b_{11}}{a} - \frac{b}{a}L \tag{3-113}$$

is the locus of points in the L-M plane that deliver a purely conductive input admittance. Values of M that exceed the right-hand side of (3-113)

correspond to a complex inductive input admittance, while smaller values of M yield capacitive complex admittances.

The power delivered to the load in the two-port network of figure (3.9) reads

$$P_o(L,M) = |V_2|^2 \mathrm{Re}(Y_L) \tag{3-114}$$

or equivalently,

$$P_o(L,M) = |V_2|^2 \mathrm{Re}\left(-\frac{I_2}{V_2}\right). \tag{3-115}$$

From figure (3.9)

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \tag{3-116}$$

and using (3-103) and (3-104),

$$\frac{I_2}{V_2} = Y_{22} - \frac{Y_{21}}{\left(\frac{Y_{21}}{2g_{22}}\right)(L + jM)}. \tag{3-117}$$

It follows that

$$\mathrm{Re}\left(-\frac{I_2}{V_2}\right) = -g_{22} + \frac{2g_{22}L}{L^2 + M^2}. \tag{3-118}$$

Substitution of (3-118) and (3-104) into (3-115) delivers

$$P_o(L,M) = P_{oo}[1 - (L - 1)^2 - M^2], \tag{3-119}$$

where

$$P_{oo} = P_o(1,0) = \frac{|Y_{21}|^2}{4g_{22}} . \qquad (3\text{-}120)$$

As portrayed in the L-M plane representation of figure (3.12), the power output surface is a paraboloid whose vortex lies at (L,M) = (1,0). Note that maximum output power for $V_1 = 1$ is realized at (L,M) = (1,0) and that (3-120) agrees with the inference that (L,M) = (1,0) is in one-to-one correspondence with a load conjugately matched to Y_{22}.

Equation (3-119) allows for a convenient definition of a passive load termination in L-M plane variables. Since $P_o(L,M)$ is nonnegative for all passive loads, the reasonable requirement that g_{22} be positive implies

$$(L - 1)^2 + M^2 \leq 1; \qquad (3\text{-}121)$$

that is, the infinitude of all possible passive load terminations maps into the closed region bounded by a unit circle centered at (L,M) = (1,0) as shown in figure (3.13). The immediate upshot of the matter is that for given load at stipulated signal frequency ω_o, (3-117) allows for computation of corresponding values for L and M. If these values simultaneously satisfy (3-111) and (3-121), the two-port network is incapable of oscillation at $\omega = \omega_o$. If, however, (3-121) is satisfied, but (3-111) is violated, a passive source termination can be found to produce oscillations at frequency ω_o.

Finally, a consideration of (3-119) reveals that the L-M plane loci of constant output powers are concentric circles centered at (L,M) = (1,0). In particular, for $P_o(L,M) = \gamma_o P_{oo}$, where γ_o is a nonnegative, less than unity, constant,

$$(L - 1)^2 + M^2 = (1 - \gamma_o). \qquad (3\text{-}122)$$

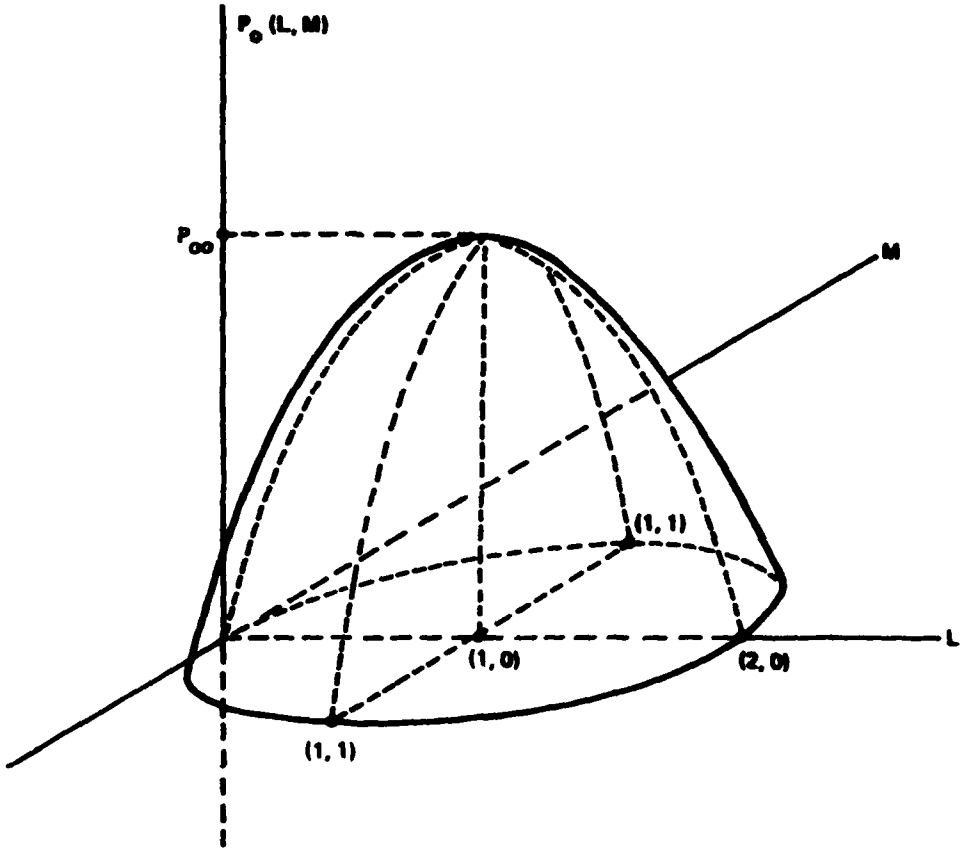


Figure (3.12). Power Output as a Function of L and M.

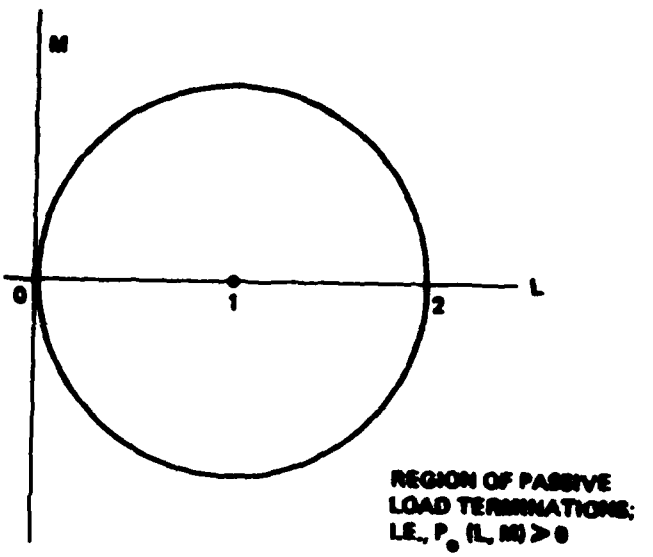


Figure (3.13). L-M Plane Operating Region Commensurate With Positive Output Power.

As depicted in figure (3.14), (3-122) is a circle at (L,M) = (1,0), having a radius of $(1 - \gamma_o)^{1/2}$. The infinitude of points lying on this circle correspond to an infinitude of load terminations which, for unity input voltage, produce an output power numerically equal to $\gamma_o P_{oo}$.

3.2.2 Power Gain in L-M Plane

Insofar as the L-M plane is concerned, the power dissipated at the input terminals is the graded plane of figure (3.10), while the power delivered to the load is the paraboloid of figure (3.12). In principle, a graphical portrayal of power gain in the L-M plane can therefore be gleaned through superposition of the $P_i(L,M)$ and $P_o(L,M)$ plots. Unfortunately, quantitative results that might be generated from an analytical pursuit of this rationale are masked by the constructional complexity inherent in three dimensional plots.

In light of the foregoing argument, consider the view looking down onto the L-M plane after superposition of the $P_i(L,M)$ and $P_o(L,M)$ curves. In figure (3.15), the unity radius circle is the base of the power output paraboloid, while the straight line represents the intersection of the power input and L-M planes. Assuming that the power input plane rises out of the page in such a way that $P_i(1,0) > 0$, the two-port network associated with figure (3.15) is unconditionally stable in the sense that $P_i(L,M) < 0$ for only those values of L and M that correspond to nonpassive loads. Finally, the circle embedded within the unity radius circle corresponds to a specific output power, $P_o(L,M)$, such that $0 \leq P_o(L,M) \leq P_{oo}$. If x is the radius of this circle, it is clear that

$$(L - 1)^2 + M^2 = x^2, \tag{3-123}$$

and (3-119) becomes

$$P_o(x) = P_{oo}(1 - x^2). \tag{3-124}$$

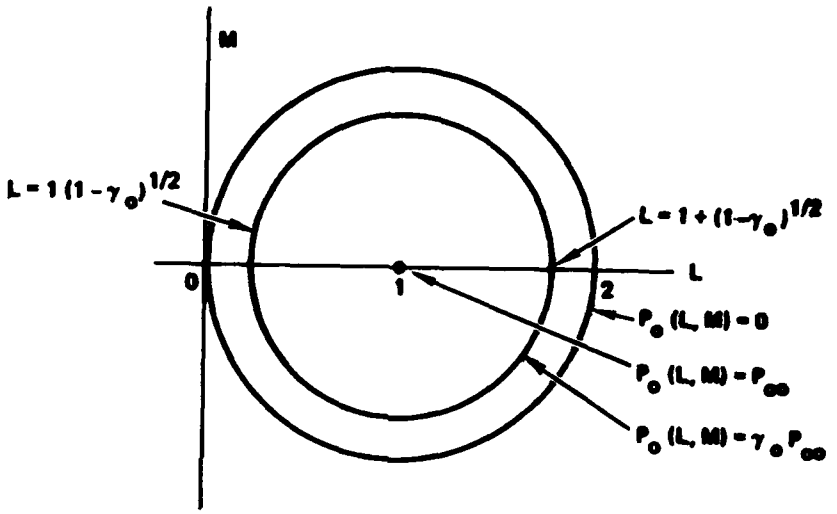


Figure (3.14). Contours of Constant Output Powers in L-M Plane.

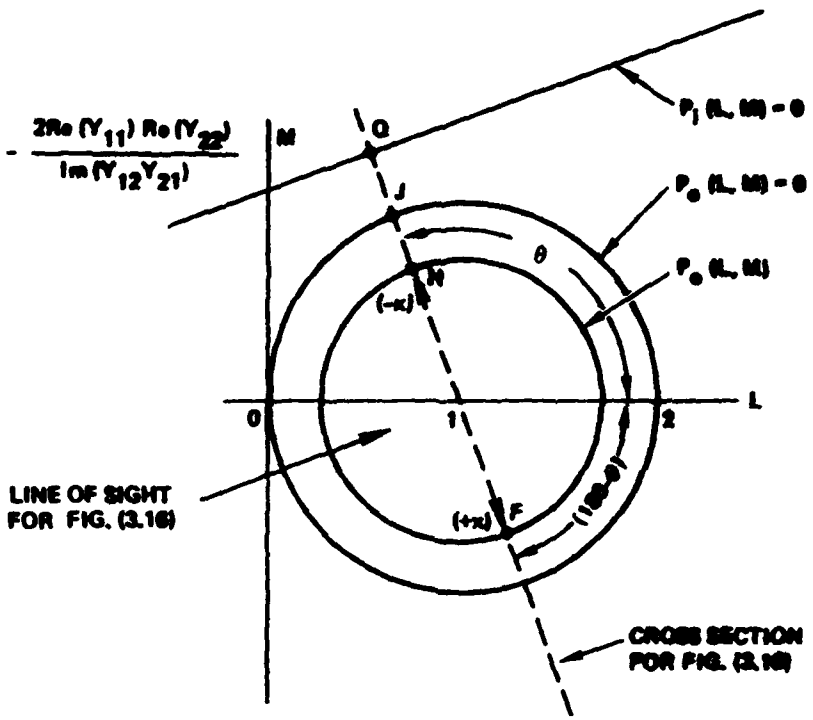


Figure (3.15). Top View of Superimposed $P_i(L,M)$ and $P_o(L,M)$ Surfaces.

Note that nonnegative output power or equivalently, a passive load termination, demands $|x| \leq 1$.

It is now profitable to focus attention on the line passing through (L,M) = (1,0) and points Q, J, H and F in figure (3.15). The line in question is perpendicular to the locus of $P_i(L,M) = 0$ at point Q. A plane containing this line and passing perpendicularly through the L-M plane cuts the cross section, as viewed along the indicated line of sight, shown in figure (3.16). Thus, if the load termination defines values of L and M that correspond to point F in the L-M plane, the power gain is the ratio of the length of the line connecting points F and D to the length of the line connecting points F and E. If, on the other hand, the load gives rise to operation at H, corresponding to negative x, the power gain is the length of line connecting H and N divided by the length of line connecting H and K.

Aside from providing a graphical interpretation of power gain in the L-M plane, the preceding geometrical manipulations suggest that the functional dependence of input power on L and M can be reduced to an equivalent dependence on a single variable, x, in much the same fashion that permits replacement of $P_o(L,M)$ by the equivalent expression, $P_o(x)$, as per (3-124). From figure (3.15), observe that

$$L = 1 + x\text{Cos}(180° - \theta) = 1 - (\text{Cos}\,\theta)x \qquad (3\text{-}125)$$

and

$$M = x\text{Sin}\,\theta. \qquad (3\text{-}126)$$

These equations do not violate (3-123) and moreover, they affix a slope of $(-\text{Tan}\,\theta)$ to the line passing through points Q, J, H, F in figure (3.15). But since the line in question is perpendicular to the locus of $P_i(L,M) = 0$, figure (3.11) provides

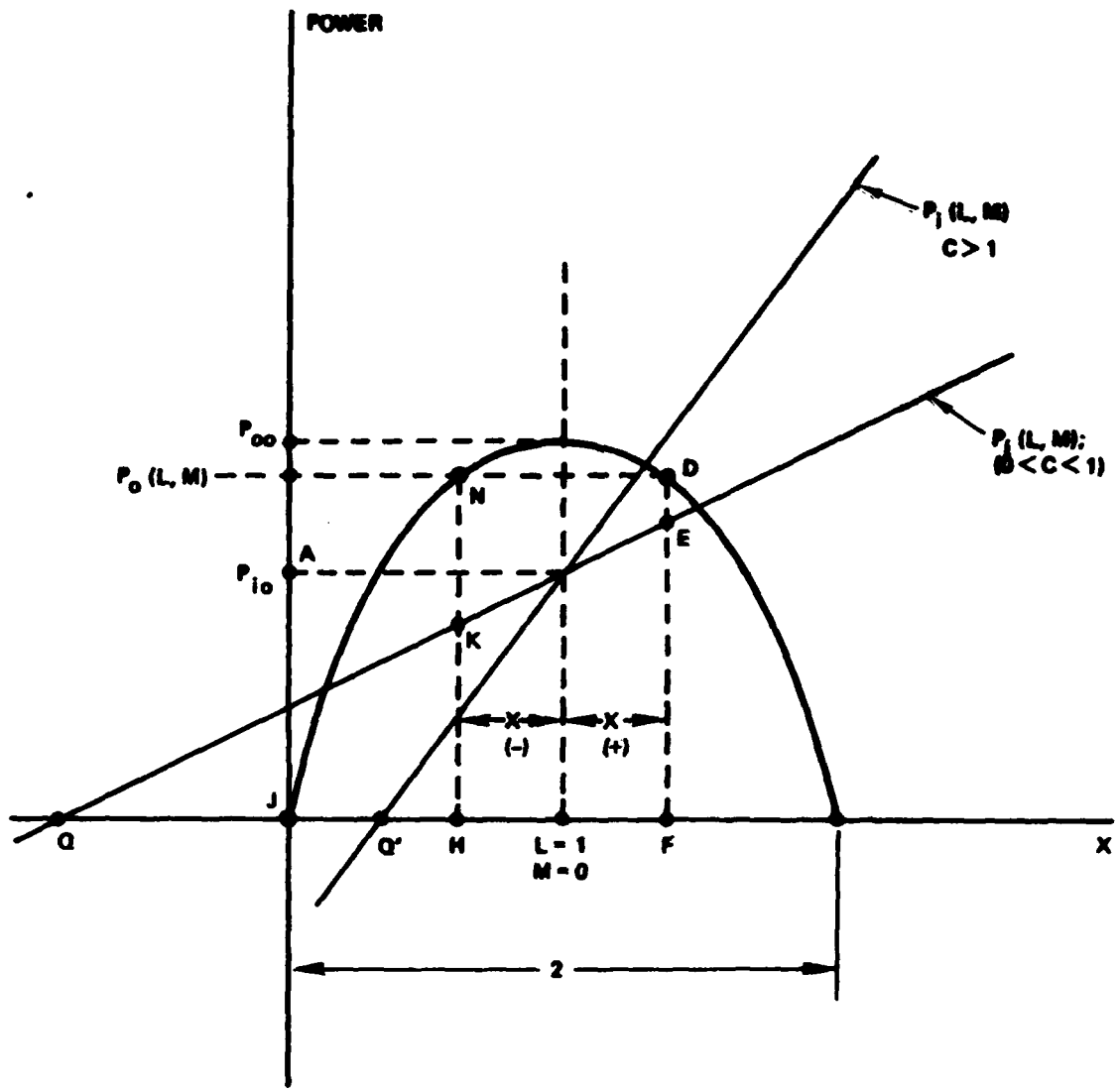


Figure (3.16). Cross-Sectional View Seen Along Indicated Line of Sight in Figure (3.15).

$$\text{Tan } \theta = \frac{\text{Im}(Y_{12}Y_{21})}{\text{Re}(Y_{12}Y_{21})} . \tag{3-127}$$

Accordingly, (3-125) through (3-127) yield

$$L = 1 - \left(\frac{\text{Re}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|}\right)x \tag{3-128}$$

and

$$M = \left(\frac{\text{Im}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|}\right)x. \tag{3-129}$$

Upon insertion of the preceding two equations into (3-110), one arrives at the simple relationship,

$$P_i(x) = P_{io}(1 + Cx), \tag{3-130}$$

where

$$P_{io} = P_i(1,0) = g_{11} - \frac{a}{2g_{22}} = \text{Re}(Y_{11}) - \frac{\text{Re}(Y_{12}Y_{21})}{2\text{Re}(Y_{22})} \tag{3-131}$$

and

$$C = \frac{(a^2 + b^2)^{\frac{1}{2}}}{2g_{11}g_{22} - a} = \frac{|Y_{12}Y_{21}|}{2\text{Re}(Y_{11})\text{Re}(Y_{22}) - \text{Re}(Y_{12}Y_{21})} . \tag{3-132}$$

From (3-124) and (3-130), it follows that the power gain is

$$G_p(x) = \frac{P_o(x)}{P_i(x)} = G_{oo}\left(\frac{1 - x^2}{1 + Cx}\right), \tag{3-133}$$

with

$$G_{oo} = \frac{P_{oo}}{P_{io}} = \frac{1}{2}C\left|\frac{Y_{21}}{Y_{12}}\right| \tag{3-134}$$

denoting a power gain commensurate with a load defined by (L,M) = (1,0).

There are a number of significant points inherent in the transformation leading to (3-133). First and most straightforwardly, it is clear that the power gain of a two-port is expressible as a function of a single independent variable, x. This variable defines a load appropriate to realization of stipulated power gain, in the sense that given x, (3-128) and (3-129) provide corresponding values of L and M, whence (3-117) can be used to define the appropriate real and imaginary parts of Y_L. In particular,

$$G_L = \mathrm{Re}(Y_L) = +g_{22}\left[\frac{2L}{L^2 + M^2}\right] - g_{22} \tag{3-135}$$

$$B_L = \mathrm{Im}(Y_L) = -b_{22} - \left(\frac{2g_{22}}{L^2 + M^2}\right)M. \tag{3-136}$$

Thus, in short, (3-133) gives power gain as an implicit function of load termination. Indeed, one may also state that $G_p(x)$ is an implicit function of input admittance since by (3-106), $Y_{in}(j\omega)$ is cast explicitly in terms of L and M. This last property is especially useful when a design requirement calls for a source termination that is conjugately matched to the network input admittance.

Assuming P_{oo} in (3-120) is positive, (3-124) confirms that all passive loads ($G_L \geq 0$) correspond to $|x| \leq 1$. Since power can be delivered to a load only when power is delivered to the input port of a stable network that couples the source to the load, a necessary condition for network stability is $P_{io} \geq 0$. From (3-131) and (3-132),

$P_{io} \geq 0$ requires nonnegative C. Now, if the input power is to be nonnegative for all nonnegative output powers, (3-130), coupled with the requirement $P_{io} \geq 0$, yields the constraint $(1 + Cx) \geq 0$ for all $|x| \geq 1$. Clearly,

$$0 \leq C \leq 1 \tag{3-137}$$

insures $P_i(x) \geq 0$ for all x such that $-1 \leq x \leq 1$. The inequality of (3-137) insures unconditional network stability in the sense that its satisfaction precludes definition of a passive load which gives rise to negative input power and hence, negative input conductance. Dissatisfaction of (3-137) implies <u>potential</u> instability; that is, at least one load can be found to generate negative input conductance. Given a negative input conductance, a source termination can be implemented to generate self-sustaining oscillations at the frequency for which Re[Yin(jω)] is negative. Equation (3-137) constitutes an extremely useful worst case stability criterion since C is a function only of two-port network parameters. Thus, (3-137) allows an evaluation of relative overall network stability prior to stipulation of source, load or power gain requirements.

The often confusing concept of potential instability in a two-port network can be clarified by considering the case of $C > 1$; that is, the case in which (3-137) is violated. Recalling (3-130), the slope of the $P_i(x)$ versus x curve depicted in figure (3.16) is CP_{io}. Thus, if $C > 1$, the x axis intercept of $P_i(x)$ lies to the right of point J in figure (3.16), thereby suggesting the existence of passive loads capable of producing negative input power or equivalently, negative input conductance. It follows that for the case of $C > 1$, the top view superimposed plot drawn in figure (3.15) is as offered in figure (3.17). The region lying above the locus of zero input power corresponds to negative input power. The part of this region that coincides with positive output power, shown crosshatched in figure (3.17), defines all passive loads that can produce oscillations. For loads that correspond to L and M values lying within the unit circle and below the locus

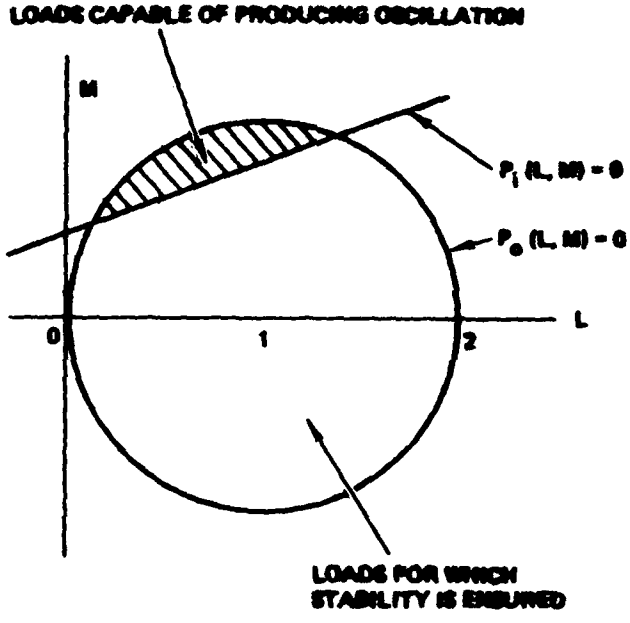


Figure (3.17). Top View of Superimposed Plots of Input and Output Power for a Potentially Unstable Two-Port.

of zero input power, the input power is positive and oscillations are precluded. Thus, the network addressed is potentially unstable, since load and corresponding source terminations can be implemented to produce oscillations. Obviously, these loads can be avoided through design procedures thoughtfully implemented to preclude operation in the indicated crosshatched area.

From (3-133), observe that $G_p(-1) = G_p(1) = 0$, which implies the existence of optimized x in the sense of maximum power gain. By straightforward utilization of differential calculus, the optimized value of x, say x_o, is

$$x_o = -\frac{1}{C} + \frac{(1 - C^2)^{\frac{1}{2}}}{C} . \tag{3-138}$$

Substitution of this result into (3-133) gives for maximum power gain,

$$G_{pm} = G_p(x_o) = \frac{2G_{oo}}{1 + (1 - C^2)^{\frac{1}{2}}} . \tag{3-139}$$

Notice that power gain can be optimized only if the utilized two-port network is unconditionally stable. This observation corroborates with the results portrayed in figure (3.16) since if $C > 1$, gain is theoretically optimized at point Q' on the x-axis. At this point, the input power is zero, the output power is finite and positive, and the power gain is infinitely large.

Since maximum power gain is realized if and only if the load is conjugately matched to the output admittance and the source is conjugately matched to the input admittance, (3-138) defines the matching requirements at input and output ports of the network in question. In essence, (3-138) is the solution to the genuinely cumbersome problem of determining the source termination which matches to an input admittance that, for nonzero internal feedback, is a function of the load termination. But the load

must be conjugately matched to the output admittance which, in turn, is a function of the unknown source termination.

3.3 Actively Peaked Broadbanding

The design of monolithic, silicon bipolar, broadbanded linear amplifiers is a significantly more difficult task than is the realization of hybrid wideband amplifiers, owing to constraints inherently imposed by the fabrication process. In particular, all monolithic fabrication processes are not readily amenable to the synthesis of efficient input, output and interstage lossless matching networks which are fundamental to state-of-the-art hybrid circuit design.

The inductors required of lossless matching networks for integrated circuits must be realized by thin film techniques. Generally speaking, matching network capacitors must also be synthesized by means of thin film, metal-on-metal (MOM) technology, since stringent interstage matching requirements at very high frequencies are rarely forgiving of the unavoidable sensitivity displayed by device junction capacity with respect to voltage. Unfortunately, thin film inductors and capacitors consume inordinately large chip area, thereby establishing the possibility of significant parasitic coupling at high signal frequencies between the energy storage element in question and other passive and active circuit elements on the chip. When combined with the invariable uncertainties in parameter values which characterize an integrated active element, this coupling virtually precludes achievement of a designable impedance transformation at circuit interstages or at circuit input and output ports.

Even if interelement coupling is negligible, integrated chip inductors are still undesirable, owing to capacitive coupling incurred between adjacent metallized spirals of the inductive coil and between the spiral lines and the substrate. This intrinsic susceptive interaction serves to limit the inductance value that can be synthesized on chip, and it also reduces the quality (Q) factor of the coil. Experiments confirm that the phenomena in question is especially troublesome

in the neighborhood of a gigahertz when (1) the number of metal spiral turns exceeds 5, (2) the width of each spiral line is less than 0.5 mils, and (3) the spacing between adjacent lines is greater than 0.25 mils.

This paper describes an alternative to interstage impedance matching as a means of monolithic broadbanding. The alternative amounts to interstage shunt peaking, wherein the required inductance is realized actively by means of an optimized common collector or common base stage.

3.3.1 Shunt-Peaked Frequency Response

Consider a lowpass amplifier whose only parasitic energy storances are capacitors and whose zeros lie at frequencies that are far in excess of the 3-decibel (dB) bandwidth of the circuit. If the amplifier is to be capable of broadbanded signal amplification, it is doubtlessly designed to deliver a dominant pole response. Accordingly, the input-to-output voltage transfer function is expressible as

$$A_o(s) \approx \frac{A_o(0)}{1 + s/B_o}, \tag{3-140}$$

where $A_o(s)$ represents the ratio of transformed voltage output, $V_o(s)$-to-transformed input voltage, $V_i(s)$, as defined in figure (3.18a). Furthermore, $A_o(0)$ is the low frequency value of voltage gain, B_o is the 3-dB radial bandwidth, and s is complex frequency. It must be stressed that $A_o(0)$ and B_o are evaluated as explicit functions of load and source terminations, R_s and R_L, respectively. As suggested in the symbolic representation of figure (3.18a) and in the corresponding model of figure (3.18b), these terminations are presumed to be purely resistive.

Let the amplifier in question drive a second circuit whose input impedance can be represented as a resistance, R_i, in shunt with a capacitance, C_i. In an attempt to improve the resultant frequency response of the loaded amplifier, shunt peaking is implemented by means of an inductance, L, in series with the output resistance, R_L. The situation

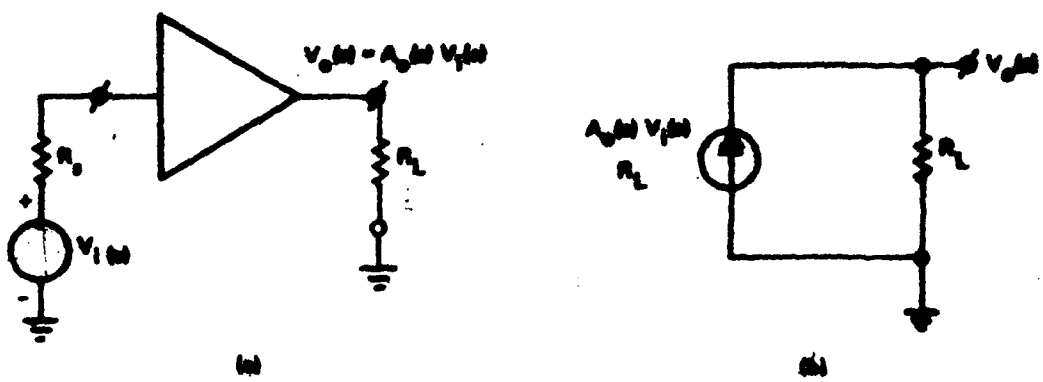


Figure (3.18). (a) Symbolic Representation of an Amplifier Having Voltage Gain, $A_o(s)$.

(b) Simplified Equivalent Circuit of Amplifier.

in question is depicted in figure (3.19). It can be shown that the transfer function, $V_L(s)/V_i(s)$, of the shunt-peaked amplifier under actual load conditions is

$$\frac{V_L(s)}{V_i(s)} = A_o(0)\left[\frac{R_i}{R_i + R_L}\right]\left\{\frac{(1 + sL/R_L)/(1 + s/B_o)}{1 + s\left[\frac{L}{R_i + R_L} + (R_i\ R_L)C_i\right] + s^2L\left(\frac{R_i}{R_i + R_L}\right)C_i}\right\}. \tag{3-141}$$

Observe that the inductor introduces two poles and a zero into the transfer characteristics.

Equation (3-141) can be cast into more useful format by appropriate algebraic substitutions and by focusing attention on the transfer function normalized to its low frequency value,

$$A_L(0) = A_o(0)\,\frac{R_i}{R_i + R_L}. \tag{3-142}$$

Letting

$$P_i \triangleq \frac{R_i}{R_i + R_L}, \tag{3-143}$$

$$\omega_N = \frac{1}{\sqrt{LP_iC_i}}, \tag{3-144}$$

$$\zeta = \frac{1}{2}\left\{\left(\frac{1 - P_i}{R_L}\right)\sqrt{\frac{L}{P_iC_i}} + R_L\sqrt{\frac{P_iC_i}{L}}\right\}, \tag{3-145}$$

the normalized transfer function or gain is

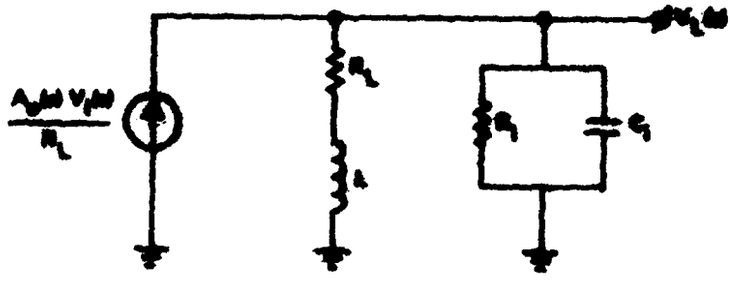


Figure (3.19). Equivalent Circuit of Shunt-Peaked Amplifier Loaded by a Circuit Whose Input Impedance is Capacitive.

$$A_{LN}(s) = \frac{(1 + sL/R_L)}{(1 + s/B_0)\left[1 + s\left(\frac{2\zeta}{\omega_N}\right) + \left(\frac{s}{\omega_N}\right)^2\right]} . \qquad (3\text{-}146)$$

Note that ζ and ω_N respectively connote damping factor and undamped natural frequency of oscillation if the zero attributed to L is made to cancel the dominant pole of the unloaded amplifier.

It should be evident that there is potential difficulty in constraining the loaded amplifier to a maximally flat magnitude response since there are two more poles than zeros. Note, however, that MFM characteristics can ostensibly be closely approximated if the basic unloaded amplifier has very large bandwidth, B_0. Unfortunately, large B_0 is an unrealistic constraint, particularly in the design of wideband circuits whose frequency capabilities are to encompass L-band spectra. Indeed, if B_0 is very large in comparison to the dominant pole frequency of the driven circuit, the need for shunt-peaked or other forms of frequency compensation applied to the driver configuration is somewhat dubious.

3.3.2 Pole-Zero Cancellation

In (3-146), let L be chosen so that the zero attributed to it cancels the dominant pole of the driver amplifier; i.e.,

$$L = R_L/B_0. \qquad (3\text{-}147)$$

Then, the normalized transfer function, expressed as an explicit function of the normalized real frequency variable,

$$y = \omega/\omega_N, \qquad (3\text{-}148)$$

is

$$A_{LN}(jy) = \frac{1}{1 - y^2 + j2\zeta y} . \qquad (3\text{-}149)$$

Figure (3.20) depicts the resultant amplifier frequency response for various values of damping factor. Clearly, severe response peaking is evidenced for small values of ζ, and in particular, it can be shown that the peak magnitude response for any value of ζ is

$$|A_p| = \frac{1}{2\zeta\sqrt{1 - \zeta^2}} . \tag{3-150}$$

This maximum magnitude response prevails at a normalized frequency given by

$$y_p = \sqrt{1 - 2\zeta^2} , \tag{3-151}$$

which is seen to be a real number if and only if $\zeta < 1/\sqrt{2}$. Since imaginary y_p constitutes a physically meaningless parameter, the stipulation, $\zeta > 1/\sqrt{2}$, is tantamount to realization of a monotonically decreasing magnitude response. In practice, most circuit design specifications call for response flatness to within only ± 3 dB over the desired passband. Setting $|A_p| \leq \sqrt{2}$ in (3-150), this design constraint translates to the relaxed damping factor requirement, $\zeta \geq 0.382$, and in turn, a number of worst case design requirements are necessarily imposed on the load.

A demonstration of the foregoing assertion requires substitution of (3-147) into (3-145) to obtain,

$$\zeta = \frac{1}{2}\left\{(1 - P_i)\left(\frac{\omega_N}{B_o}\right) + \left(\frac{B_o}{\omega_N}\right)\right\}. \tag{3-152}$$

The damping factor is a minimum, say ζ_{MIN}, when

$$\frac{B_o}{\omega_N} = \sqrt{1 - P_i} , \tag{3-153}$$

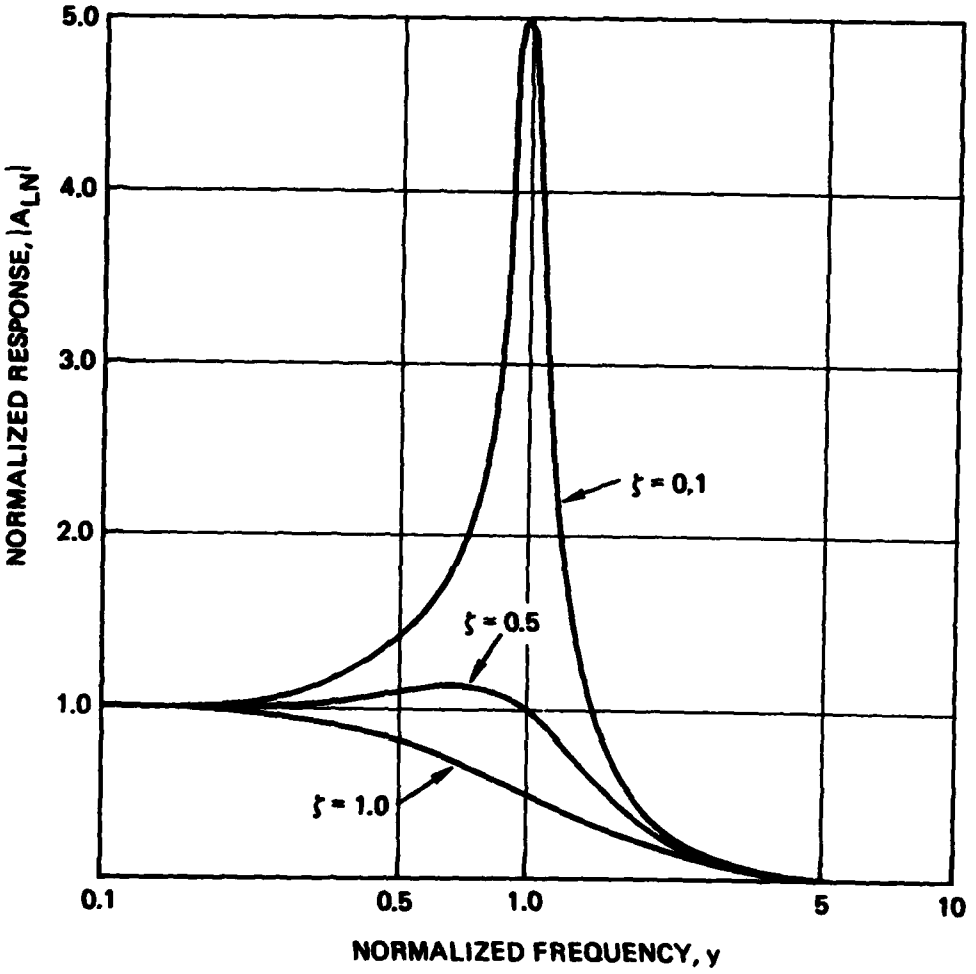


Figure (3.20). Amplifier Frequency Response for the Case of Pole-Zero Cancellation in (3-146).

for which

$$\zeta_{MIN} = \sqrt{1 - P_i} \,. \tag{3-154}$$

In order to preclude excessive response peaking, one may insure $\zeta \geq 0.382$ by requiring $\zeta_{MIN} \geq 0.382$, whence $P_i \leq 0.854$ or by (3-143),

$$R_i \leq 5.853\, R_L. \tag{3-155}$$

With $P_i \leq 0.854$, (3-153), (3-147) and (3-144) combine to deliver

$$(R_L \| R_i) C_i \geq 0.146/B_o. \tag{3-156}$$

Now, if L were to be set to zero in figure (3.19), the resultant 3-dB bandwidth, say B_D, assuming pole dominance and recalling (3-140), can be approximated by

$$B_D \approx \frac{1}{\frac{1}{B_o} + (R_L \| R_i) C_i} \,. \tag{3-157}$$

Because of (3-156), this approximation gives rise to the inequality,

$$B_o \geq 1.146\, B_D. \tag{3-158}$$

Inequalities (3-155) and (3-156) are the sufficient, but non-necessary conditions for realization of a frequency response whose peak magnitude is within 3-dB of the low frequency amplifier gain, provided shunt peaking is utilized to cancel the dominant pole of the unloaded driver amplifier. Equation (3-155) asserts that the input resistance of the driven stage can be no larger than approximately 5.85 times the load resistance associated with the driver. On the other hand, (3-158) implies that the unloaded bandwidth of the driver must be at least 14.6% larger than the bandwidth obtained in the absence of shunt peaking

when the driver is coupled to the succeeding stage. Both inequalities are pragmatic design tools in the sense that R_i, B_o, and B_D can be straightforwardly estimated by means of computer-aided analyses.

3.3.3 Approximate Maximally Flat Magnitude (AMFM)

Returning to (3-146), it is easily shown that

$$|A_{LN}(jy)|^2 = \frac{1 + (\omega_N L/R_L)^2 y^2}{1 + y^2\left\{\left(\frac{\omega_N}{B_o}\right)^2 - 2(1 - 2\zeta^2)\right\} + y^4\left\{1 - 2\left(\frac{\omega_N}{B_o}\right)^2(1 - 2\zeta^2)\right\} + y^6\left(\frac{\omega_N}{B_o}\right)^2}, \quad (3\text{-}159)$$

where (3-148) is utilized. If the term involving y^6 is negligibly small at all frequencies through the immediate neighborhood of the overall circuit bandwidth, an AMFM response is produced if

$$\left(\frac{\omega_N L}{R_L}\right)^2 = \left(\frac{\omega_N}{B_o}\right)^2 - 2(1 - 2\zeta^2). \quad (3\text{-}160)$$

Using (3-144) and (3-145), (3-160) gives rise to an inductance value which reads

$$L = R_L^2 C_i\left(\frac{P_i}{2 - P_i}\right)\left\{-1 + \left\{1 + \left(\frac{2 - P_i}{P_i}\right)\left[1 + \left(\frac{1}{B_o P_i R_L C_i}\right)^2\right]\right\}^{1/2}\right\}. \quad (3\text{-}161)$$

Observe that for the special case defined by

$$\left.\begin{aligned} P_i &\approx 1 \\ B_o P_i R_L C_i &>> 1 \end{aligned}\right\}, \quad (3\text{-}162)$$

(3-161) simplifies considerably to

$$L \approx R_L^2 C_i \{-1 + (1 + 1)^{\frac{1}{2}}\} \approx 0.414 R_L^2 C_i . \qquad (3\text{-}163)$$

The assumption, $P_i \approx 1$, implies that the driven stage does not impose an appreciable low frequency load on the driver network. On the other hand, the presumed inequality above suggests that the pole established by the input port of the driven stage in the absence of shunt peaking is significantly larger than the 3-dB bandwidth of the unloaded driver stage. Regardless of whether or not (3-162) is valid, (3-160) reduces (3-159) to

$$|A_N(jZ)|^2 = \frac{1 + Q_o^2 Z^2}{1 + Q_o^2 Z^2 + \left\{\left(\frac{B_o}{\omega_N}\right)^4 - (1 - Q_o^2)\right\} Z^4 + \left(\frac{B_o}{\omega_N}\right)^4 Z^6} , \qquad (3\text{-}164)$$

where

$$Z = \omega / B_o \qquad (3\text{-}165)$$

is signal frequency normalized to the 3-dB bandwidth of the unloaded driver stage with no shunt peaking and

$$Q_o = \frac{B_o L}{R_L} \qquad (3\text{-}166)$$

is the effective quality factor of inductance L at frequency B_o.

In order to achieve an AMFM response, two conditions must be satisfied. First, the denominator on the right-hand side of (3-164) must be a Hurwitz polynomial in argument Z^2[8] and second, the term involving Z^6 in this characteristic polynomial must be negligibly small throughout the frequency range of interest. The Hurwitz condition is

satisfied if $Q_o^2 \geq 1$, while a sufficient condition which guarantees the second constraint for all frequencies through the immediate neighborhood of the overall 3-dB circuit bandwidth is

$$\left(\frac{B_o}{\omega_N}\right)^4 Z_B^6 << 1. \tag{3-167}$$

In (3-167), Z_B is the overall circuit bandwidth normalized to B_o and thus,

$$|A_N(jZ_B)|^2 = 1/2. \tag{3-168}$$

Note that $Z_B > 1$ is a prudent necessity since if $Z_B \leq 1$, the actual circuit bandwidth is less than that realized prior to shunt peak compensation. It follows that a necessary condition for satisfaction of (3-167) is

$$B_o/\omega_N < 1. \tag{3-169}$$

Figure (3.21) exemplifies the nature of (3-164) for the special case of $B_o/\omega_N = 0.5$. Two observations are immediately apparent. First, the sensitivity of frequency response with respect to effective quality factor decreases markedly as Q_o is made to increase. Indeed, (3-164) demonstrates that the compensated normalized circuit bandwidth is always unity in the limit as Q_o is made very large since if (3-167) is satisfied,

$$\lim_{Q_o \to \infty} |A_N(j1)|^2 = \frac{1 + Q_o^2}{1 + 2Q_o^2} \approx \frac{1}{2}$$

Second, broadbanded response is achieved for small Q_o, despite dissatisfaction of (3-167). For the case of $Q_o = 1$, figure (3.21) shows $Z_B = 2$, whence the left-hand side of the inequality in (3-167) is $(1/2)^4(Z_B^6) = 4$.

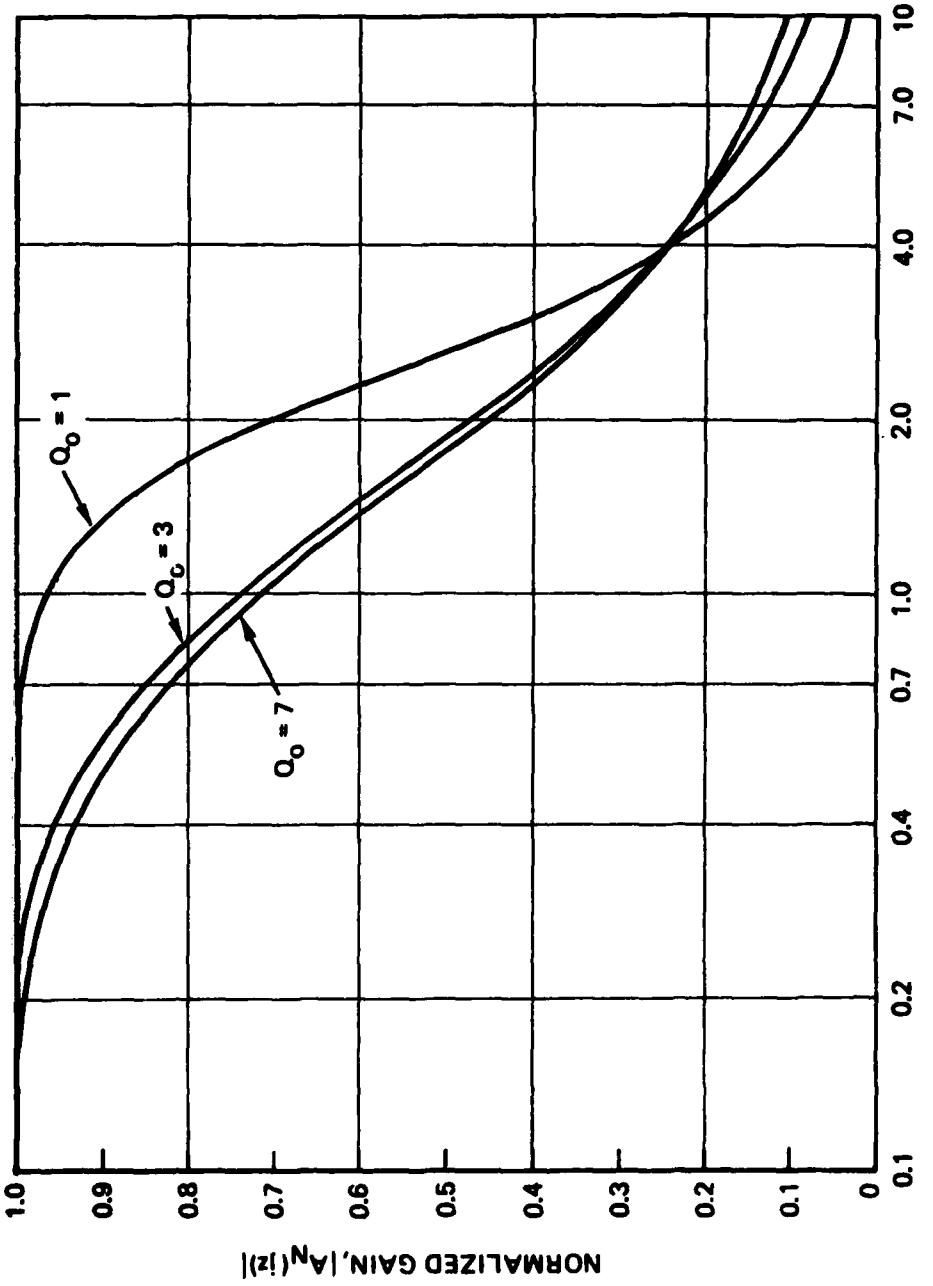


Figure (3.21). AMFM Frequency Responses for $B_o/\omega_N = 1/2$.

The case of $Q_o = 1$ is especially interesting in view of the facts that $Q_o = 1$ maximizes 3-dB bandwidth and $Q_o \geq 1$ is required to insure that the denominator polynomial on the right-hand side of (3-164) is Hurwitz; that is, $Q_o \geq 1$ precludes a peaked response in the circuit passband. It is easily shown that (3-168) is satisfied for $Q_o = 1$ if $Z_B = (\omega_N/B_o)$. Thus, the maximum attainable bandwidth for the compensated circuit is

$$B_{MAX} = \omega_N, \tag{3-170}$$

where ω_N is stipulated by (3-144) and L in (3-144) is given by (3-161).

3.3.4 Inductor Realization

The foregoing analyses and discussion are rendered germane to monolithic circuit design if the properties indigenous to the impedance seen looking into the emitter of a bipolar junction transistor are exploited to synthesize the required inductance. This impedance, which is symbolically represented as $Z_E(s)$ in figure (3.22), can be approximated by a simple linear resistance, say R_E, in series with a frequency invariant inductance, say L_E, provided that the signal frequencies of interest are not excessively large [9]. In particular, let ω_β be the transistor beta cutoff frequency and define ω_1 and ω_2 such that

$$\omega_1 = \frac{1}{(r_B + R_X + r_c + R_c)C_{Tc}} \tag{3-171}$$

and

$$\omega_2 = \frac{1}{(r_c + R_c)C_{Tc}}. \tag{3-172}$$

In (3-171) and (3-172), r_B is the net low frequency base resistance of the device, r_c is the low frequency collector resistance, and C_{Tc} is the effective collector-base capacitance. Then for $(\omega/\omega_1)^2 << 1$ and

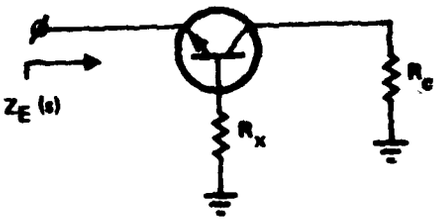


Figure (3.22). AC Schematic Diagram of Circuit Employed to Synthesize an Inductor Actively.

$\omega^2/\omega_2\omega_\beta << 1$,

$$R_E \approx \frac{1}{g_m} + \frac{r_B + R_x}{h_{fe} + 1} + r_e, \tag{3-173}$$

$$L_E \approx \left(\frac{\omega_\beta + \omega_2}{\omega_\beta \omega_2}\right)\left(\frac{r_B + R_x}{h_{fe} + 1}\right) + \frac{1}{g_m \omega_1} + \frac{(r_c + R_c)\|(r_B + R_x)}{\omega_1}, \tag{3-174}$$

where g_m is the small-signal, common-emitter transconductance, r_e is the intrinsic emitter resistance, and h_{fe} is the small-signal, short-circuit, common-emitter current gain.

Figure (3.23) displays the AC schematic diagram of a simple common emitter amplifier (Q1) which is shunt peaked compensated by virtue of the active inductance circuit (Q2). With respect to the systems model of figure (3.19) $A_o(s)$ is the gain of transistor Q1 when the output port is unloaded and when the collector of Q1 is loaded by a resistance, $R_L = R_{LE} + R_E$. This gain easily derives from a judicious computer simulation, wherein R_E is estimated by way of (3-173) or is gleaned from a complimentary computer-oriented analysis of the low frequency input impedance associated with the Q2 stage. More definitively, one wishes to establish $A_o(s)$ in light of $L_E = 0$ and in turn, the value of R_E commensurate with $L_E = 0$ is conveniently obtained by defaulting all frequency domain parameters in the computer model of Q2 to insiginficant proportions. This is to say that all junction and substrate capacitances are set to zero, neutral base transit time is made to vanish, and so forth. Upon establishment of the simulated frequency response, $|A_o(j\omega)|$, $A_o(0)$ and B_o in (3-140) are straightforwardly deduced and for given output load termination, (3-143) through (3-145) are evaluated with L set to L_E.

It is evident that the simple circuit in figure (3.23) can be viewed as a dynamic half circuit of a differential amplifier. Accordingly, differential shunt peaking is also plausible, as suggested by figure (3.24).

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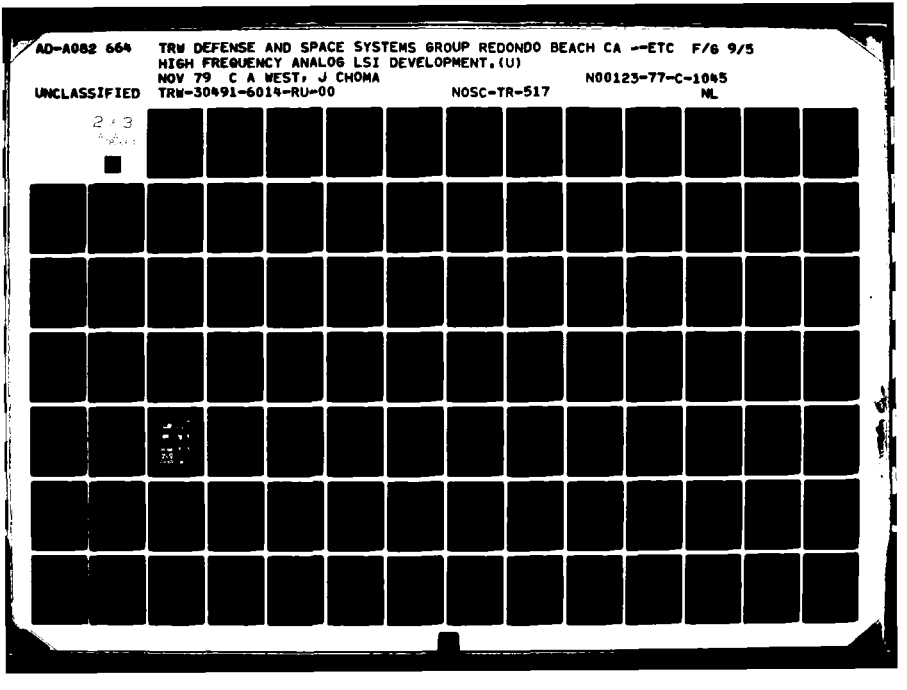

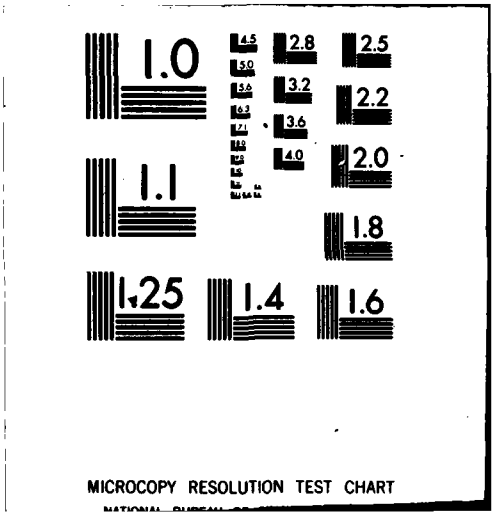
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MICROCOPY RESOLUTION TEST CHART

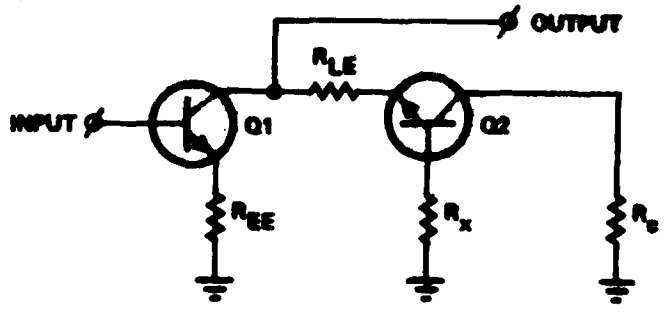


Figure (3.23). Common Emitter Amplifier (Q1) Shunt Peaked by Active Emitter Impedance of Q2. Biasing network is not shown.

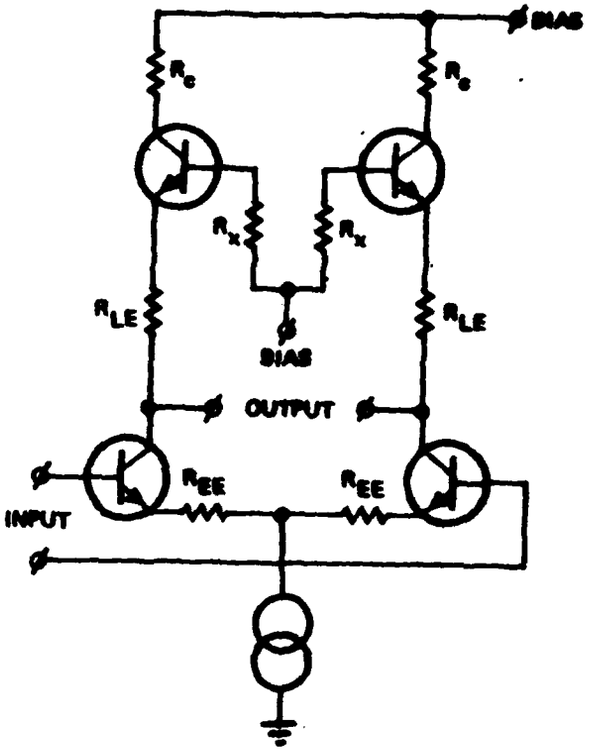


Figure (3.24). Differential Realization of Circuit Shown in Figure (3.23).

3.3.5 A Design Exercise

Assume that the transistors in figure (3.24) are biased to deliver $h_{fe} = 45$, $\omega_\beta = 2\pi$ (100 MHz), $r_B = 140$ ohms, $r_c = 70$ ohms, $r_e = 3$ ohms, $g_m = 160$ ms, and $C_{Tc} = 0.10$ pF. Assume further that $B_o = 2\pi$ (780 MHz) when $R_{LE} = 75$ ohms and $R_x = 1000$ ohms. Note that R_x must be known or estimated in order to evaluate R_L and hence, B_o. Finally, let the entire configuration be designed for as flat and as broad a passband as possible when the load termination is 500 ohms in shunt with 0.1 pF.

Using (3-173), $R_E = 34.03$ ohms, whence $R_L = R_{LE} + R_E = 109.03$ ohms. For $R_i = 500$ ohms, $R_L = 109.03$ ohms, and $C_i = 0.1$ pF, P_i in (3-143) is 0.82 and by (3-161), the required inductance is $L_E = 21.82$ nH. From (3-170) and (3-144), the best possible bandwidth is $B_{MAX} = 2\pi$ (3.76 GHz), which is realized only if $Q_o = 1$. However, (3-166) yields $Q_o = 0.981$. This quality factor cannot be substantially increased through suitable adjust of R_x, and hence R_L, since in (3-161) the product, $B_o P_i R_L C_i$ is very small. In particular, $B_o P_i R_L C_i = (43.87)(10^{-3})$ in this example and accordingly, (3-161) delivers

$$Q_o = \frac{B_o L}{R_L} \approx (B_o R_L C_i)\left(\frac{P_i}{2 - P_i}\right)\left(\frac{2 - P_i}{P_i}\right)^{\frac{1}{2}} \frac{1}{B_o R_L C_i P_i} = \frac{1}{\sqrt{P_i(2 - P_i)}},$$

which is virtually independent of R_L, particularly since P_i is reasonably close to unity. Thus, an AMFM response cannot be ensured and an alternate design approach is mandated.

The alternative design methodology is pole-zero cancellation, which in effect forces $Q_o = 1$ within the constraint of hopefully minimal peaking in the frequency response. From (3-147), $L = L_E = 22.25$ nH and by (3-144), $\omega_N = 2\pi$ (3.72 GHz). Using (3-152), $\zeta = 0.53$, which is larger than the minimally acceptable damping factor of 0.382. Equation (3-150) predicts a magnitude response peak of $|A_p| = 1.11 = 0.91$ dB, which occurs at a frequency of 2.45 GHz, where (3-151) and (3-148) have been invoked.

Using (3-149), the predicted bandwidth of the compensated circuit corresponds to $y = 1.237$ or with $\omega_N = 2\pi$ (3.72 GHz), the bandwidth is 4.60 GHz.

It is a simple matter to verify that (3-174) delivers $L_E \approx 22.25$ nH if $R_x = 380$ ohms and $R_c = 0$. Recall that $R_x = 1000$ ohms is initially presumed. The revised value of R_x provides $R_E = 20.55$ ohms and hence $R_L = 95.55$ ohms, as opposed to the originally estimated value of $R_L = 109.03$ ohms. This 12% "error" in estimated R_L is doubtlessly inconsequential in view of inevitable device parameter uncertainties and bandwidth (B_o) estimation errors attributed to approximations implicit in the computer-based models for all bipolar devices.

From (3-171) and (3-172), $\omega_1 = 2\pi$ (2.70 GHz) and $\omega_2 = 2\pi$ (22.74 GHz). At a frequency equivalent to the estimated compensated bandwidth of 4.60 GHz, $\omega^2/\omega_2\omega\beta = 9.31$ and $(\omega/\omega_1)^2 = 2.90$, and therefore, both of the requirements, $(\omega/\omega_1)^2 << 1$ and $\omega^2/^2{}_2{}^2\beta << 1$, are violated. This situation intimates that the actual bandwidth realized can be expected to be less than 4.60 GHz. Indeed, a computer simulation of the circuit addressed herewith verifies a 3-dB bandwidth of approximately 1.12 GHz. Although this performance is far short of the 4.60 GHz computation, it nonetheless represents a 44% improvement in the original (uncompensated) bandwidth of 780 MHz.

4.0 CIRCUIT DEVELOPMENT

4.1 Voltage Reference Supply

During the course of designing a monolithic analog RFLSI circuit, there invariably arises a need to generate a voltage reference that sustains an appropriate thermal coefficient. In an earlier contractual document [10], the circuit shown in figure (4.1) is proposed to satisfy a broad variety of such needs, since a component of the desired reference voltage, V_I, turns out proportional to a thermally sensitive base-emitter junction bias voltage. In this circuit, I_L represents the current drained by the load driven by the reference supply, while resistor ratios R_1/R_2 and R_s/R_p determine the desired thermal coefficient. Voltage V_I is necessarily positive in figure (4.1), but it should be clear that if R_s is returned to a negative supply, V_I can be positive, negative or even zero.

For large DC beta and reasonable load current, I_L,

$$V_I \approx \left(\frac{R_s}{R_s + R_p}\right)V_{CC} + \left(\frac{1 + R_1/R_2}{1 + R_s/R_p}\right)V_{BE1} - V_{BE2}. \qquad (4\text{-}1)$$

If the base-emitter junction voltages have thermal coefficients at any convenient reference junction temperature, T_o, which are identical and equal to

$$\left.\frac{\partial V_{BE1}}{\partial T}\right|_{T_o} \equiv \left.\frac{\partial V_{BE2}}{\partial T}\right|_{T_o} \triangleq K_{BE}, \qquad (4\text{-}2)$$

the thermal coefficient of voltage V_I is seen to be

$$\left.\frac{\partial V_I}{\partial T}\right|_{T_o} = \left\{\frac{1 + R_1/R_2}{1 + R_s/R_p} - 1\right\}K_{BE}. \qquad (4\text{-}3)$$

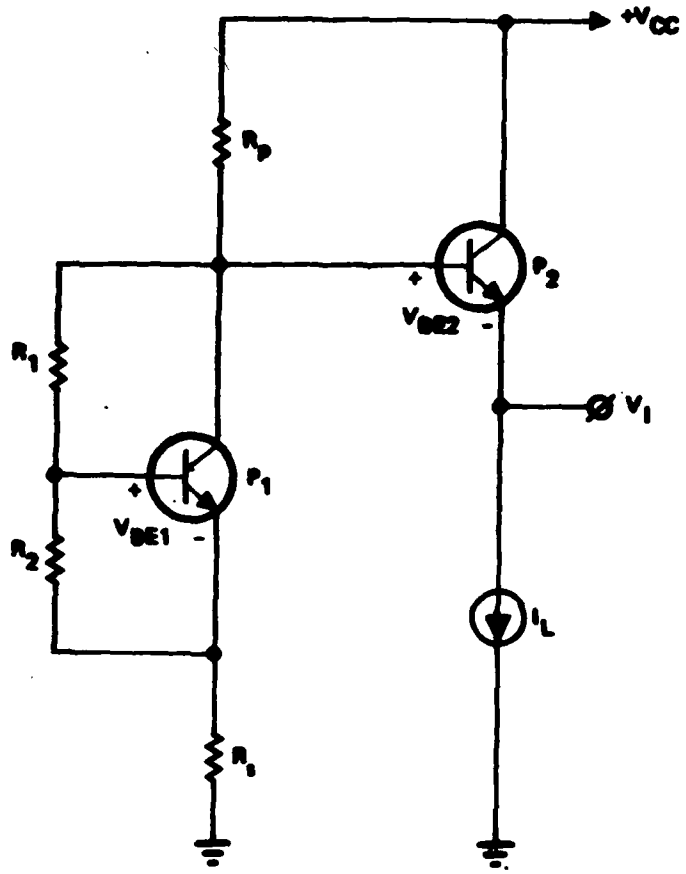


Figure (4.1). Basic Voltage Reference Circuit

If, for example, this coefficient is to be rendered equal to K_{BE}, the coefficient pertinent to one forward biased junction voltage drop,

$$\frac{R_1}{R_2} = 1 + \frac{2R_s}{R_p}, \tag{4-4}$$

and (4-1) collapses to

$$V_I \approx \left(\frac{R_s}{R_s + R_p}\right)V_{CC} + 2V_{BE1} - V_{BE2}. \tag{4-5}$$

A definitive thermal analysis of the proposed voltage reference circuit is a worthwhile undertaking, since (4-4) presumably ensures a prescribed thermal coefficient at but a single temperature, T_o. To commence the investigation, recall that the emitter current of a bipolar junction transistor is closely approximated by

$$I_E(T) \approx I_s(T)e^{V_{BE}(T)/V_T} \tag{4-6}$$

where V_T is the familiar kT/q and I_s is related to temperature by [11]

$$I_s(T) = I_{ss}\left(\frac{T}{T_o}\right)^n e^{[V_{BE}(T) - V_{go}]/V_T}, \tag{4-7}$$

with $V_{BE}(T)$ connoting the base-emitter junction bias commensurate with the flow of emitter current in the amount of $I_E(T)$ at temperature T. In practice, however, the dependence of this emitter current on temperature is determined in part by circuitry connected peripherally to the device in which $I_E(T)$ is monitored. If the dependence of I_E on temperature is modeled as a power law relationship of the form,

$$I_E(T) = I_E(T_o)\left(\frac{T}{T_o}\right)^{\lambda}, \tag{4-9}$$

(4-6), (4-7) and (4-9) combine to deliver

$$V_{BE}(T) = V_{go} + V_T LN\left[\frac{I_E(T_o)}{I_{ss}}\right] + (\eta - \lambda)V_T LN\left(\frac{T}{T_o}\right) \qquad (4\text{-}10)$$

or equivalently

$$V_{BE}(T) = V_{go} - \frac{T}{T_o}\left[V_{go} - V_{BE}(T_o)\right] + \frac{(\eta - \lambda)kT}{q} LN\left(\frac{T}{T_o}\right). \qquad (4\text{-}11)$$

It follows that

$$\frac{\partial V_{BE}(T)}{\partial T} = -\frac{V_{go} - V_{BE}(T_o)}{T_o} - \frac{k}{q}\left\{1 + (\eta - \lambda)LN\left(\frac{T}{T_o}\right)\right\}, \qquad (4\text{-}12)$$

while

$$\frac{\partial^2 V_{BE}(T)}{\partial T^2} = -\frac{k}{q}\left(\frac{\eta - \lambda}{T}\right). \qquad (4\text{-}13)$$

The first order temperature coefficient at temperature T_o is thus seen to be

$$K_{BE} \triangleq \left.\frac{\partial V_{BE}(T)}{\partial T}\right|_{T_o} = -\frac{k}{q}\left\{1 + \frac{V_{go} - V_{BE}(T_o)}{V_{To}}\right\} \qquad (4\text{-}14)$$

and the second order thermal coefficient is

$$\left.\frac{\partial^2 V_{BE}(T)}{\partial T^2}\right|_{T_o} = -\frac{k}{q}\left(\frac{\eta - \lambda}{T_o}\right), \qquad (4\text{-}15)$$

where in (4-14)

$$V_{To} = \frac{kT_o}{q} . \tag{4-16}$$

Observe that two identical bipolar devices display the same first order temperature coefficient at a given reference temperature if and only if both devices sustain identical forward biases across their base-emitter junctions. On the other hand, two identical bipolar devices exude the same second order temperature coefficient at reference temperature T_o if and only if the presumed power law dependence on temperature of their emitter currents is identical.

Returning to the basic supply circuit of figure (4.1), let it be assumed that at temperature T_o, the base-emitter bias voltages of P1 and P2 are identical. The output voltage can thus be designed to provide a voltage,

$$V_I = \left(\frac{R_s}{R_s + R_p}\right) V_{CC} + K_o V_{BE}, \tag{4-17}$$

where

$$\frac{R_1}{R_2} = K_o + (K_o + 1)(R_s/R_p). \tag{4-18}$$

From (4-3) and (4-14), the first order temperature coefficient is

$$\left.\frac{\partial V_I}{\partial T}\right|_{T_o} = -\frac{kK_o}{q}\left\{1 + \frac{V_{go} - V_{BE}(T_o)}{V_{To}}\right\}. \tag{4-19}$$

It is to be understood that K_o need not be integral: rather, it is chosen so that the temperature coefficient defined by (4-19) matches

the requirements imposed by the load circuit across which V_I is developed. Using (4-1), the second order temperature coefficient is

$$\left.\frac{\partial^2 V_I}{\partial T^2}\right|_{T_o} = (K_o + 1)\left.\frac{\partial^2 V_{BE1}}{\partial T^2}\right|_{T_o} - \left.\frac{\partial^2 V_{BE2}}{\partial T^2}\right|_{T_o}$$

$$= -\frac{k}{qT_o}\left\{(\lambda_2 - \lambda_1) + K_o(\eta - \lambda_1)\right\}, \qquad (4\text{-}20)$$

where (4-15) has been exploited. If the load current, I_L, in figure (4.1) is thermally stabilized, $\lambda_2 = 0$ in (4-20), and the second order coefficient becomes

$$\left.\frac{\partial^2 V_I}{\partial T^2}\right|_{T_o} = -\frac{k}{qT_o}\left\{K_o\eta - (K_o + 1)\lambda_1\right\}. \qquad (4\text{-}21)$$

Clearly, it is possible for this term to vanish. Moreover, the above coefficient is comparable to the second order temperature coefficient realized in most classical bandgap references sources [12]. Indeed, the magnitude of (4-21) is actually less than the magnitude of the second order temperature coefficient ideally achieved in bandgap reference configurations, provided

$$K_o < \frac{\eta + \lambda_1 - 1}{\eta - \lambda_1}. \qquad (4\text{-}22)$$

4.2 Level Shifting

An ideal level shifting circuit is an interstage network capable of translating its quiescent input voltage to a lesser quiescent output voltage without incurring small-signal transfer function attenuation. Both passive and active level shifting can be accomplished monolithically,

although, as might be expected, each method can only approximate desired level shift attributes over somewhat restricted operational environments.

The simplest passive level shifter is the coupling capacitor, which obviously gives rise to significant signal attenuation at low frequencies. Three other disadvantages are evidenced when coupling capacitors are utilized in OAT RFLSI circuits. First, OAT metal-on-metal (MOM) capacitors consume inordinately large chip area. A MOM capacitance of only 4 picofarads consumes an amount of area that is virtually two orders of a magnitude greater than that required of a typical OAT bipolar device. Second, considerable signal attenuation is evidenced at moderate-to-high frequencies as a result of an unavoidable parasitic capacitance that appears between one terminal of the coupling capacitance and ground. Typically, attenuations in the range of 35%-to-50% are produced and since the value of the parasitic is quite sensitive to OAT oxide characteristics, the precise amount of attenuation can rarely be predicted a priori, in advance of circuit fabrication. Finally, a coupling capacitor restricts circuit designer freedom in the sense that the translated quiescent level is necessarily zero. There are, unfortunately, numerous occasions when nonzero translated levels are required for efficient biasing of subsequently cascaded circuits.

An active level shifting circuit, such as that shown in figure (4.2), obviates most of the difficulties indigenous to MOM coupling capacitors. The circuit is simple, consumes minimal chip area, and generally achieves a voltage attenuation that is less than 15% for frequencies that approach L-band. A disadvantage is that unlike the coupling capacitor, the circuit at hand consumes quiescent power.

4.2.1 DC Analysis

Assuming both transistors in figure (4.2) sustain a base-emitter junction bias of V_{BE} and have identical static current gains in the amount of h_{FE}, base current I_{B2} is

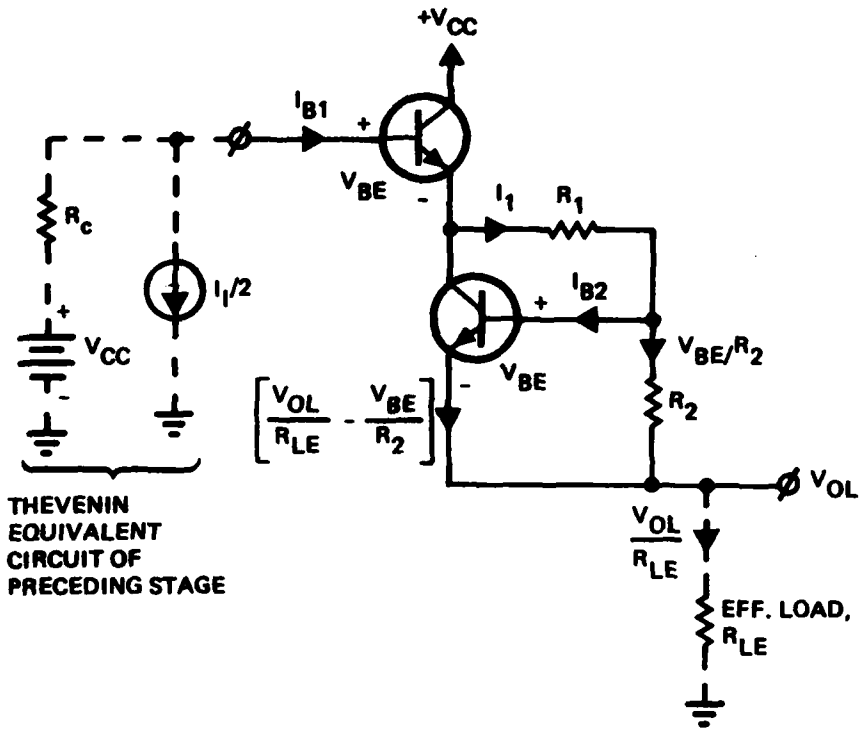


Figure (4.2). Level Shifting Circuit. Equivalent source and load circuits shown pertain to quiescent operating conditions.

$$I_{B2} = \left(\frac{V_{OL}}{R_{LE}} - \frac{V_{BE}}{R_2}\right)/(h_{FE} + 1)$$

and current I_1 reads

$$I_1 = \frac{V_{OL}}{(h_{FE} + 1)R_{LE}} + \left(\frac{h_{FE}}{h_{FE} + 1}\right)\frac{V_{BE}}{R_2} .$$

Base current I_{B1} is thus

$$I_{B1} = \left(\frac{1}{h_{FE} + 1}\right)\left\{h_{FE}I_{B2} + I_1\right\} = \frac{V_{OL}}{(h_{FE} + 1)R_{LE}} .$$

It follows that

$$V_{CC} - \frac{R_c I_I}{2} = \frac{R_c V_{OL}}{(h_{FE} + 1)R_{LE}} + V_{BE}$$

$$+ R_1\left\{\frac{V_{OL}}{(h_{FE} + 1)R_{LE}} + \left(\frac{h_{FE}}{h_{FE} + 1}\right)\frac{V_{BE}}{R_2}\right\} + V_{BE} + V_{OL}$$

$$= V_{OL}\left\{1 + \frac{R_c + R_1}{(h_{FE} + 1)R_{LE}}\right\} + V_{BE}\left\{2 + \left(\frac{h_{FE}}{h_{FE} + 1}\right)\frac{R_1}{R_2}\right\}. \qquad (4\text{-}23)$$

Noting that $(V_{CC} - R_c I_I/2)$ is the quiescent open circuit voltage, say V_{OC}, applied to the level shifter, and taking $h_{FE} >> 1$, the amount of DC translation is seen to be

$$V_{OC} - V_{OL} \approx \frac{(R_c + R_1)V_{OL}}{(h_{FE} + 1)R_{LE}} + \left(2 + \frac{R_1}{R_2}\right)V_{BE} , \qquad (4\text{-}24)$$

which is seen to be somewhat dependent on the actual output voltage. This undesirable dependence can be somewhat neutralized by modifying the basic level shifter to obtain the alternate shifting scheme proposed in figure (4.3).

In the circuit of figure (4.3),

$$I_{E1} = I_1 + h_{FE}I_{B2} - \frac{V_{BE}}{R_3} = \frac{V_{OL}}{R_{LE}} - \frac{V_{BE}}{R_3},$$

$$I_{B3} = \left(\frac{1}{h_{FE}+1}\right)\left\{\frac{V_{BE}}{R_3} + \frac{I_{E1}}{(h_{FE}+1)}\right\}$$

$$= \left(\frac{1}{h_{FE}+1}\right)\left\{\left(\frac{h_{FE}}{h_{FE}+1}\right)\left(\frac{V_{BE}}{R_3}\right) + \frac{V_{OL}}{(h_{FE}+1)R_{LE}}\right\}.$$

Then

$$V_{OC} = I_{B3}R_c + 3V_{BE} + R_1I_1 + V_{OL}$$

$$= V_{OL}\left\{1 + \frac{R_1 + R_c/(h_{FE}+1)}{(h_{FE}+1)R_{LE}}\right\}$$

$$+ V_{BE}\left\{3 + \left(\frac{h_{FE}}{h_{FE}+1}\right)\left[\frac{R_1}{R_2} + \frac{R_c}{(h_{FE}+1)R_3}\right]\right\}. \qquad (4\text{-}25)$$

For

$$\left.\begin{aligned} \frac{R_1}{R_2} &>> \frac{R_c}{(h_{FE}+1)R_3} \\ R_1 + \frac{R_c}{h_{FE}+1} &<< (h_{FE}+1)R_{LE} \\ h_{FE} &>> 1 \end{aligned}\right\}, \qquad (4\text{-}26)$$

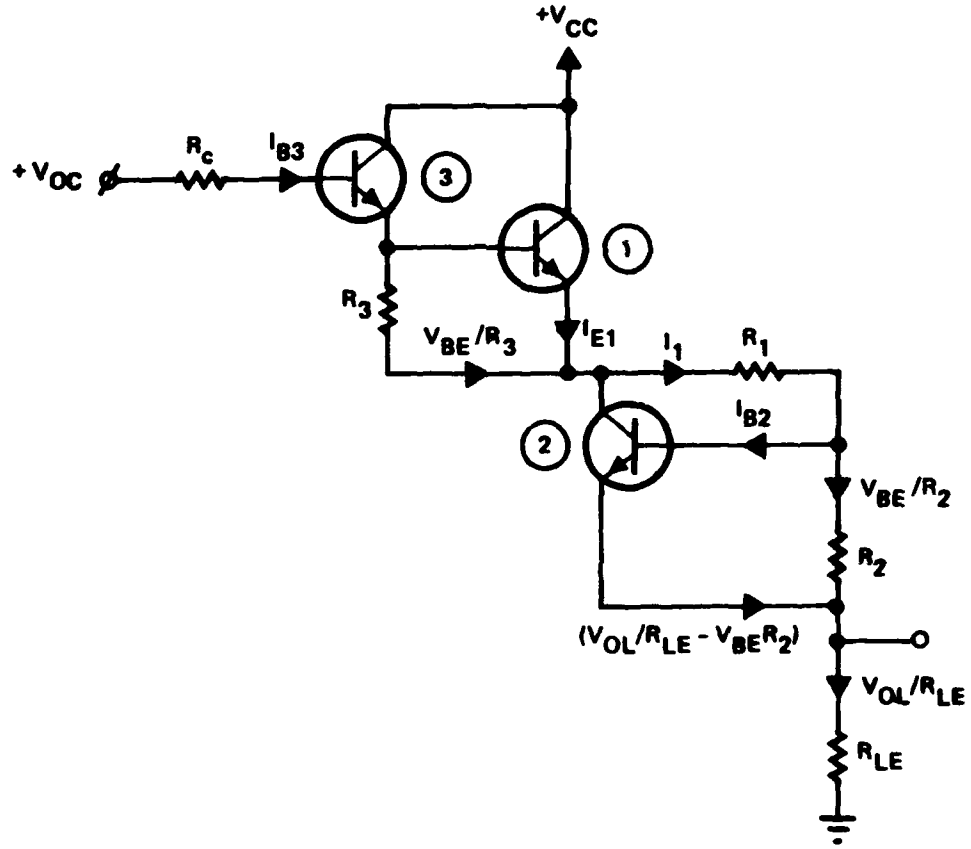


Figure (4.3). Level Shifter With Modified Darlington Input.

$$V_{OC} - V_{OL} \approx \left(3 + \frac{R_1}{R_2}\right) V_{BE} ; \tag{4-27}$$

that is, the amount of level shift is essentially independent of the output voltage.

4.2.2 Small-Signal Analysis

The approximate low frequency small-signal model for the modified level shifting configuration is shown in figure (4.4). Assuming identical transistors having identical small-signal parameters and if

$$\left.\begin{aligned} (\beta_o + 1)R_2 &>> r_B + R_{pi} \\ (\beta_o + 1)R_3 &>> r_B + R_{pi} \end{aligned}\right\}, \tag{4-28}$$

a straightforward circuit analysis confirms an open circuit voltage gain, A_o of

$$A_o = \left.\frac{V_o}{V_i}\right|_{R_{LE} = \infty} = 1. \tag{4-29}$$

Moreover, the short-circuit or Thevenin output resistance, R_T, is

$$R_T = \left(\frac{1}{\beta_o + 1}\right)\left\{R_1\left[1 + \frac{r_B + R_{pi}}{R_3}\right] + 2(r_B + R_{pi})\right\}$$

$$+ \frac{1}{(\beta_o + 1)^2}\left\{\left[1 + \frac{r_B + R_{pi}}{R_3}\right]\left[R_c + r_B + R_{pi}\right]\right\}, \tag{4-30}$$

where

$$\beta_o \triangleq g_m R_{pi} \tag{4-31}$$

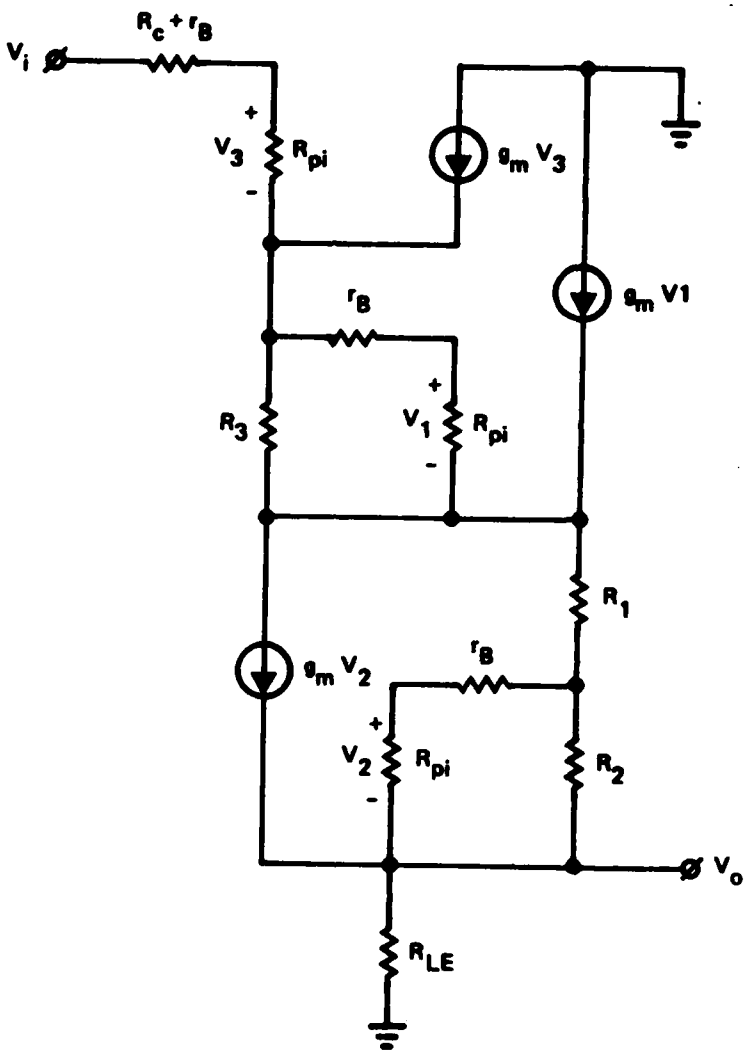


Figure (4.4). Small-Signal Equivalent Circuit of Modified Level Shifter.

is the small-signal short-circuit device current gain at low frequencies. Observe that R_T is almost completely independent of effective source resistance, R_c. Typically one can realistically expect $R_T \leq 100$ ohms.

4.3 Differential-to-Single-Ended Converter

Design procedures aimed toward fabricating a direct coupled linear integrated circuit capable of amplifying high frequency input voltages invariably exploit the numerous advantages afforded by differential circuit technology. If the circuit undergoing design is destined to drive an active or passive load whose input port cannot be excited differentially, provisions must be made to transform the differential output signal of the amplifier in question to an appropriate single-ended output voltage.

The simplest type of differential-to-single-ended converter is the resistively loaded emitter coupled pair [13] schematically portrayed in figure (4.5). In this circuit, the desired single-ended output voltage, v_o, is extracted from only one of the two collectors which establish the differential output voltage, v_{do}. A disadvantage of this circuit is unacceptable sensitivity of v_o to the common mode input signal, v_{ci}. A second drawback is profoundly serious in view of the difficulty encountered in achieving moderately large voltage gains at very high frequencies. In particular, since $v_o = v_{do}/2$ under balanced conditions, a factor of two in gain is sacrificed merely in the process of transforming the differential output signal to single-ended format.

A commonly employed converter is the emitter coupled pair with active pnp collector loads shown in figure (4.6) [14]. While this circuit exudes excellent common mode rejection characteristics, the large low frequency dynamic resistance of transistor Q_4 virtually precludes superior high frequency performance. Moreover, the high frequency response of the circuit in figure (4.6) is substantially worse than a first order circuit analysis might predict, since custom integrated circuit fabrication processes rarely produce both npn and pnp transistors

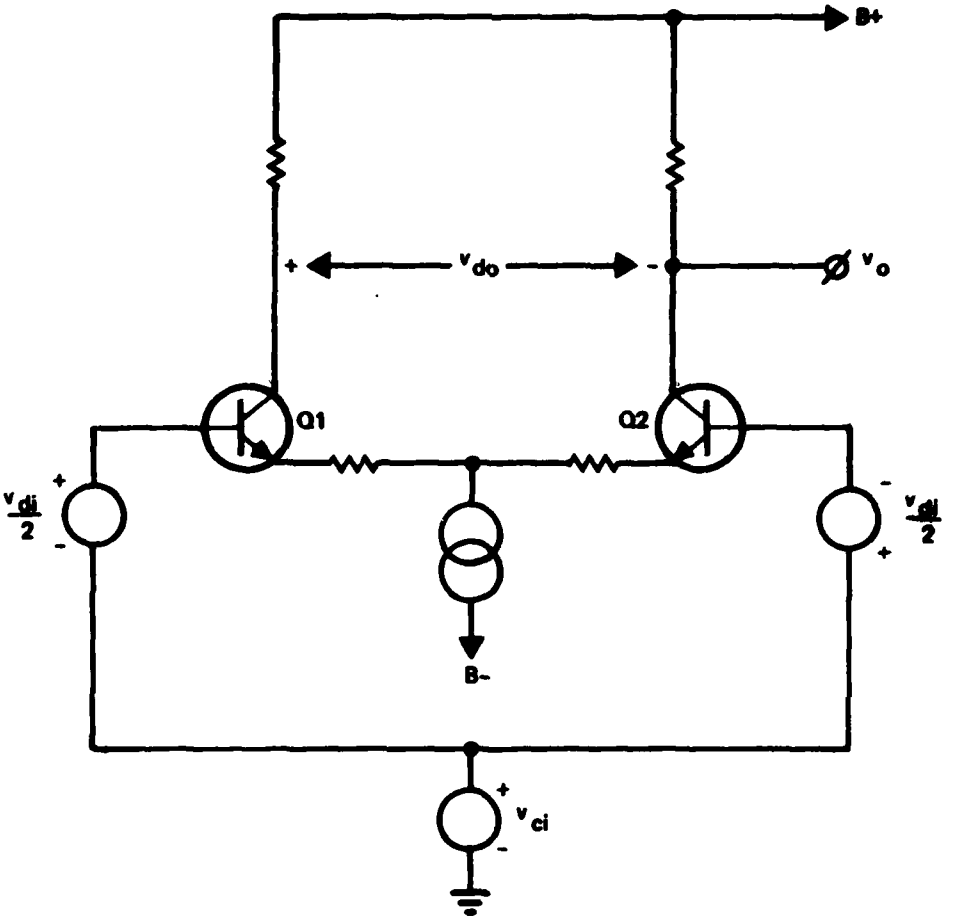


Figure (4.5). Resistively Loaded Emitter-Coupled Differential Amplifier.

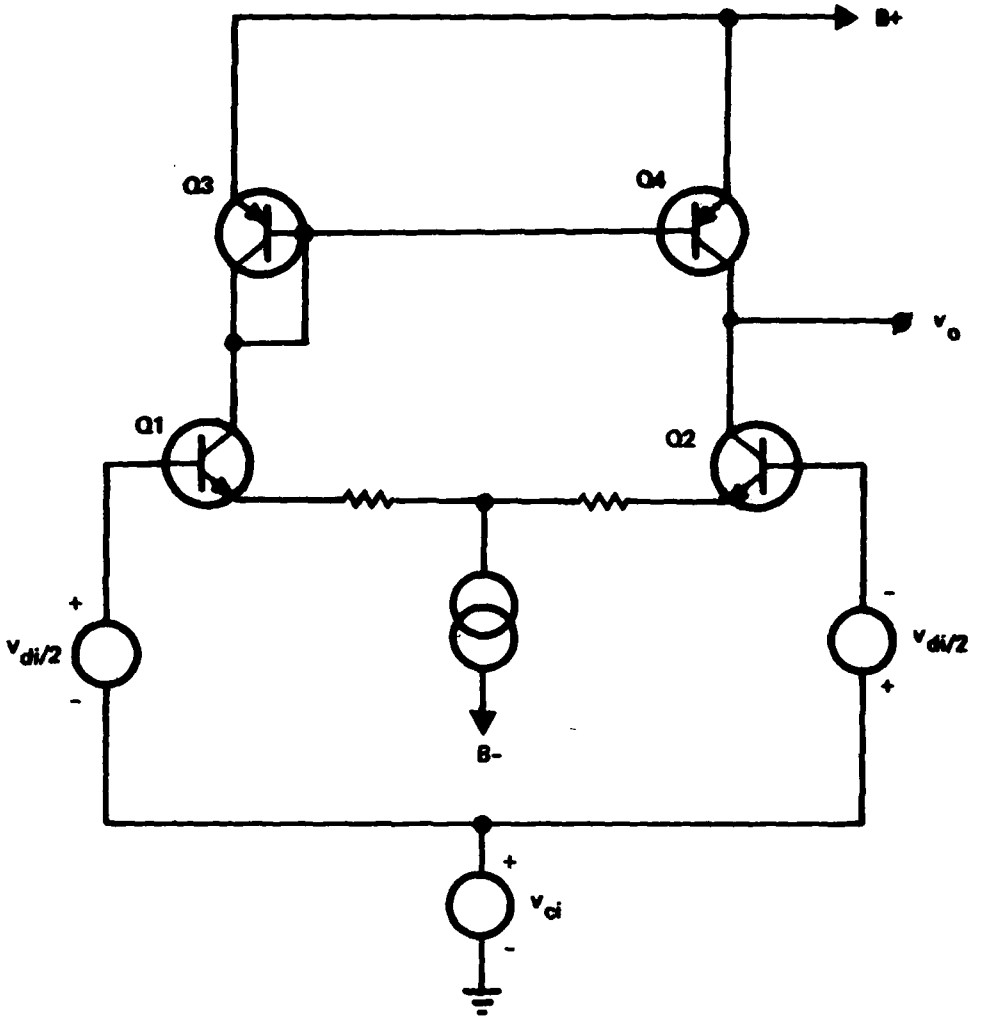


Figure (4.6). Actively Loaded Emitter Coupled Differential Amplifier.

having excellent high frequency response capabilities. The OAT high frequency process is geared toward realization of high quality npn devices only and thus, OAT RFLSI circuit designers must, for all intents and purposes, resign themselves to pnp transistor nonexistence.

The converter described and analyzed herein utilizes only npn transistors, has a single ended output voltage-to-differential input voltage conversion ratio that is nearly 0 dB, and displays 3 dB bandwidths that approach 60% of the short circuit gain-bandwidth product of the transistors embedded in the proposed converter.

4.3.1 NPN Converter

The proposed differential-to-single-ended converter assumes the basic schematic form offered in figure (4.7), where R_{s1} and R_{s2} are effective Thevenin resistances associated with signal sources v_{s1} and v_{s2}, respectively. Voltages V_{sQ1} and V_{sQ2}, which are likely to derive directly from a preceding stage whose differential open circuit output voltage, $(v_{s1} - v_{s2})$, is to be converted to the single-ended output signal, v_o, bias the converter to ensure linearized operation. In general, V_{sQ1} and V_{sQ2} are not identical.

Assume for the moment that $R_{E1} = R_{E2} = 0$ and that signals v_{s1} and v_{s2} simultaneously increase; i.e., a common mode excitation component prevails at each of the two inputs. An increase in v_{s1} produces an increase in the emitter current of diode-connected transistor Q1, and this increasing current is mirrored by an increase in the emitter current of Q2. In turn, the increase in Q2 emitter current spawns a decrease in the collector-emitter voltage of Q2. Optimal circuit operation is achieved if this decrease in collector-emitter voltage offsets most of the increase in common mode input voltage so that v_o is rendered nearly insensitive to common mode signal excitation.

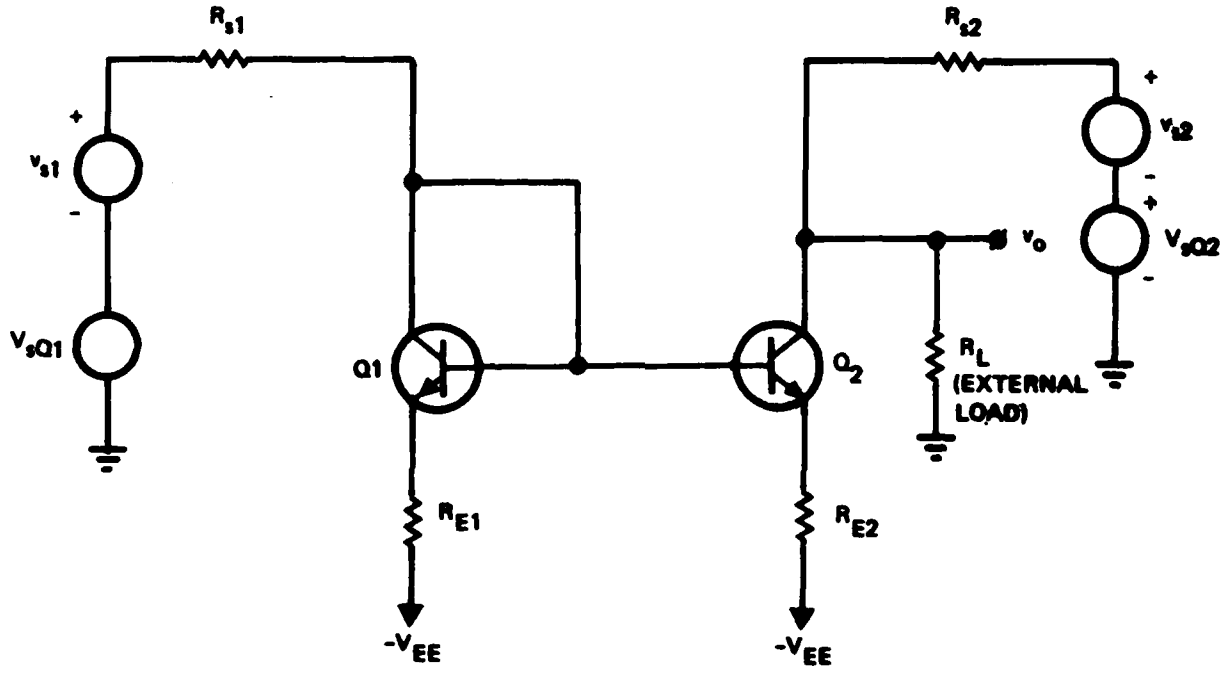


Figure (4.7). Basic Schematic Diagram of Differential-to-Single Ended Converter.

4.3.2 Small-Signal Analysis

The foregoing qualitative considerations can be cast into quantitative form through analysis of the small-signal low frequency equivalent circuit given in figure (4.8). In this circuit, the hybrid-pi models of Q1 and Q2 in figure (4.7) reflect both the possibility that these devices conduct dissimilar quiescent currents and the obvious fact that the quiescent collector-base voltages of Q1 and Q2 must differ if saturation of Q2 is to be precluded. Accordingly, base resistances r_{B1} and r_{B2}, short circuit common emitter current gains β_1 and β_2, and base-emitter junction diffusion resistances $r_{\pi 1}$ and $r_{\pi 2}$ are permitted to differ. Moreover, R'_{E1} and R'_{E2} differ from R_{E1} and R_{E2}, respectively, in the basic schematic diagram by an amount equal to the intrinsic emitter resistance of each transistor.

It can be shown that for $\beta_2 >> 1$, the converter output voltage is

$$v_o = \left(\frac{R_L}{R_L + R_{s2}}\right)\left\{v_{s2} - \frac{R_{s2}v_{s1}}{\frac{R_{s1}}{\beta_2} + \left(\frac{R'_{E2} + h_{ib2}}{R'_{E1} + h_{ib1}}\right)(R'_{E1} + R_{s1} + h_{ib1})}\right\}, \quad (4\text{-}32)$$

where

$$h_{ibj} \triangleq \frac{r_{Bj} + r_{\pi j}}{\beta_j + 1} \quad (4\text{-}33)$$

is the common base short circuit input resistance of the jth transistor. Clearly, infinite common mode rejection ratio results if the coefficient of v_{s1} within the bracketed quantity on the right-hand side of (4-32) is unity; that is,

$$R_{s2} = \frac{R_{s1}}{\beta_2} + \left(\frac{R'_{E2} + h_{ib2}}{R'_{E1} + h_{ib1}}\right)(R'_{E1} + R_{s1} + h_{ib1}). \quad (4\text{-}34)$$

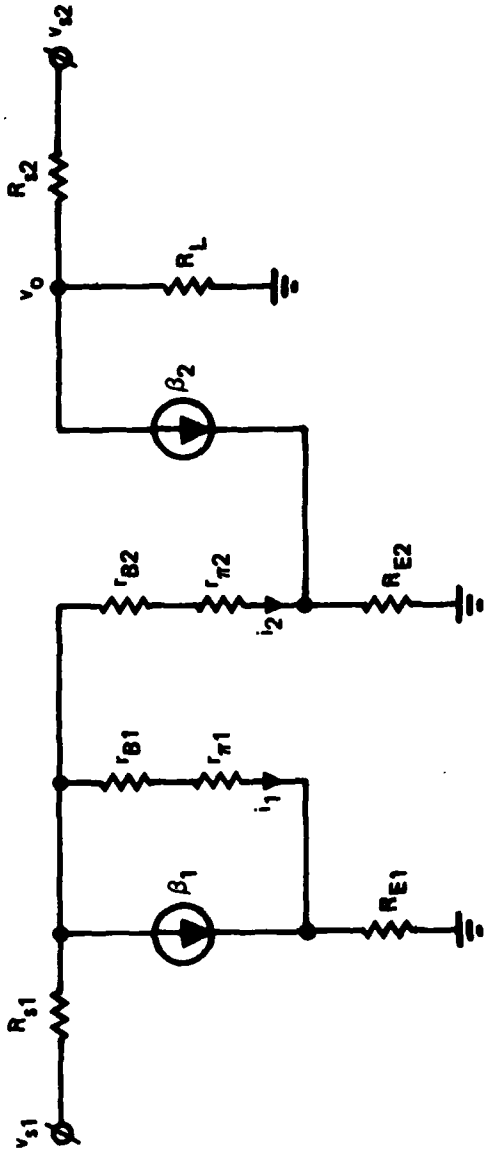


Figure (4.8). Small-Signal, Low Frequency Equivalent Circuit of Converter Given in Figure (4.7).

An effective way of satisfying (4-34) is to force $R'_{E1} << h_{ib2}$ by setting $R_{E1} = R_{E2} = 0$ in figure (4.7). Then for $h_{ib2} \approx h_{ib1}$ and large β_2,

$$R_{s2} \approx h_{ib2} + R_{s1}, \tag{4-35}$$

which suggests that the effective Thevenin resistance of the signal source driving the collector of the output transistor be made larger than the Thevenin resistance of the other signal source by an amount equal to h_{ib2}. Since h_{ib} is in general the nominal forward biased terminal resistance of a diode-connected transistor, the design constraint imposed by (4-35) is realized by inserting a diode in series with the collector of Q2. This assertion presumes that (1) the inserted diode has electrical characteristics that are identical to Q2, and (2) the Thevenin source resistances associated with v_{s1} and v_{s2} are identical.

The situation at hand is depicted in figure (4-9), where R_{E1} and R_{E2} in the original configuration have been set to zero. Assuming $h_{ib1} \approx h_{ib2} \triangleq h_{ib}$, letting the Thevenin source resistances be denoted by R_s, and assuming that Q1 and Q2 have identical intrinsic emitter resistances, say r_e, the resultant differential mode gain and common mode rejection ratio are as follows:

$$A_{DM} \triangleq \frac{v_o}{v_{s2} - v_{s1}} \approx \left(\frac{R_L}{R_L + R_s + h_{ib}}\right)\left\{\frac{R_s + h_{ib} + r_e/2}{R_s + h_{ib} + r_e}\right\}; \tag{4-36}$$

$$CMRR \triangleq \frac{A_{DM}(v_{s1} + v_{s2})}{2v_o} \approx \frac{R_s + h_{ib} + r_e/2}{r_e + R_s/\beta_2}. \tag{4-37}$$

In (4-36) and (4-37), β_2 is presumed to be significantly larger than unity.

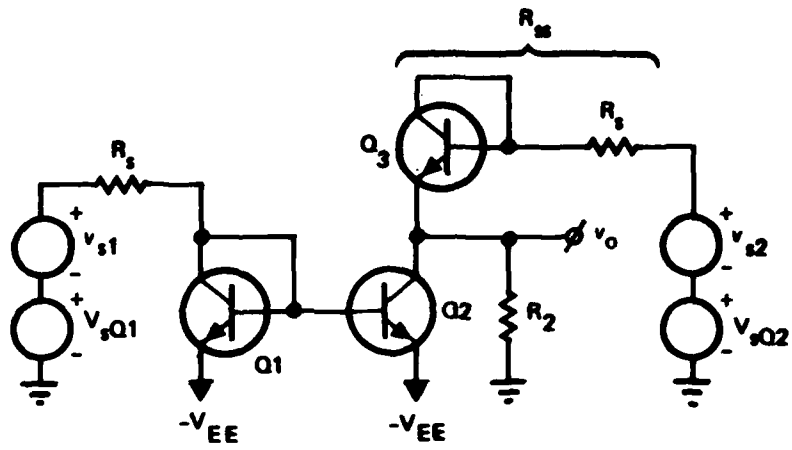


Figure (4.9). Differential-to-Single Ended Converter Optimized for Maximal Common Mode Rejection Ratio.

The circuit configured in figure (4.9) was subjected to a SPICE small-signal computer-aided analysis. A modified Gummel-Poon model was utilized for each of the three transistors, whose parameters reflect the bipolar characteristics of a nominal 5 GHz OAT process. In the simulation, $v_{sQ1} = 0$, $V_{EE} = 0.8$ volt, $V_{sQ2} = 1.6$ volts, and $R_1 = R_2 = 50$ ohms. Load resistor R_L is made infinitely large in order to permit convenient assessment of the differential frequency response of the basic converter cell. The resultant collector current flowing in each transistor is approximately 3.90 mA, the collector-emitter voltage of Q1 and Q3 is 747 mV, the collector-emitter voltage of Q2 is 1.37 volts, and the common emitter short circuit gain-bandwidth product for each device is nominally 3.2 GHz.

Figure (4.10) is the simulated differential frequency response. The low frequency gain is greater than -0.25 dB, and the three-decibel bandwidth is greater than 1.8 GHz. Note that even at 2.5 GHz, the conversion gain is approximately 1.5 dB larger than the low frequency gain provided by the simple converter of figure (4.5). The indicated bandwidth turns out to be almost an order of a magnitude larger than the bandwidth produced by the alternative converter shown in figure (4.6) if transistors comparable to these embedded in the proposed converter are used.

4.4 Negative Resistance Gain Cell

The realization of extremely high voltage gain over moderately broad passbands with OAT RFLSI technology is a nontrivial design problem owing to the inavailability of high quality pnp bipolar devices. As a result, the use of pnp current source loads, as used ubiquitously in the majority of commonly available operational amplifiers, is precluded.

A plausible solution to the problem at hand is the all npn circuit depicted in figure (4.11). Current sources I_0 and I_I flow through dynamic resistances R_0 and R_I, respectively, both of which are presumably large. Voltage V_{di} is the differential input signal, V_{ci} symbolizes the common mode input excitation, and the differential

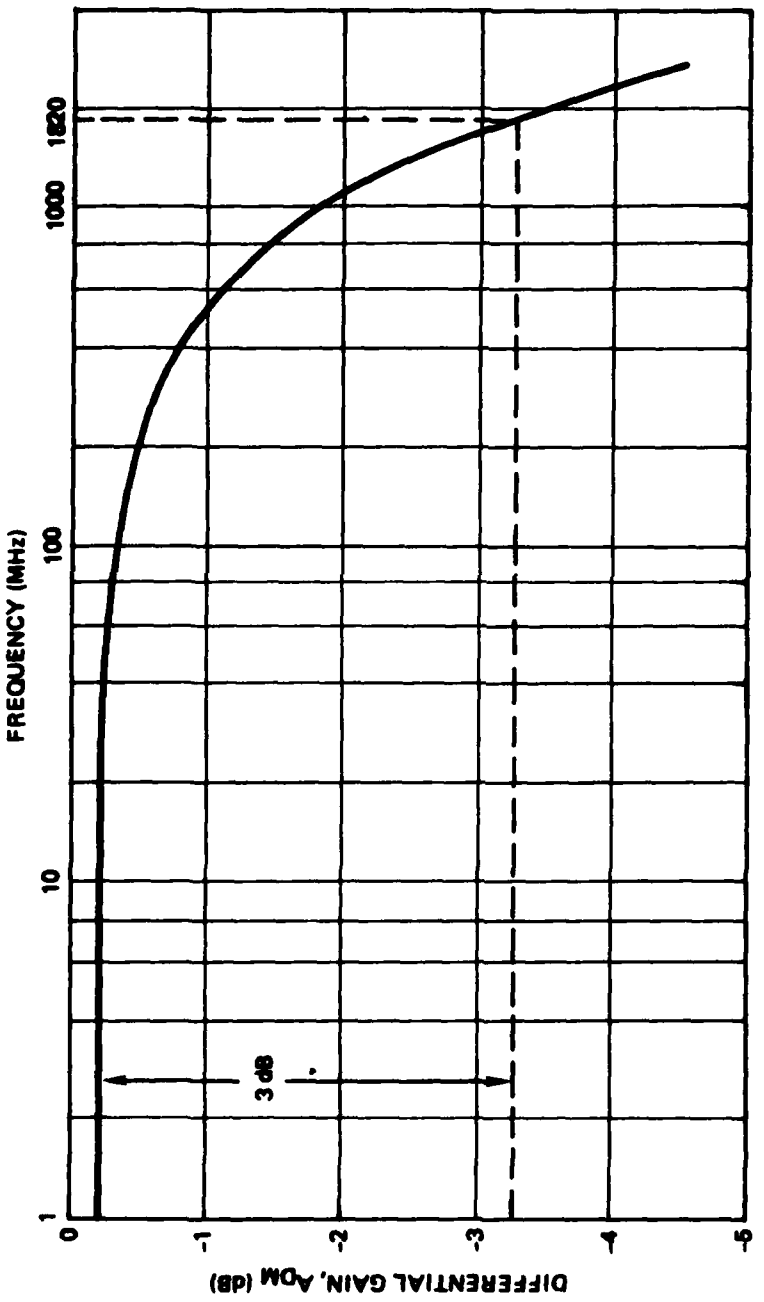


Figure (4.10). Frequency Response for Converter in Figure (4.9) for $V_{SQ1} = 0$, $V_{EE} = 0.8$ Volt, $V_{SQ2} = 1.6$ Volts, $R_1 = R_2 = 50$ Ohms.

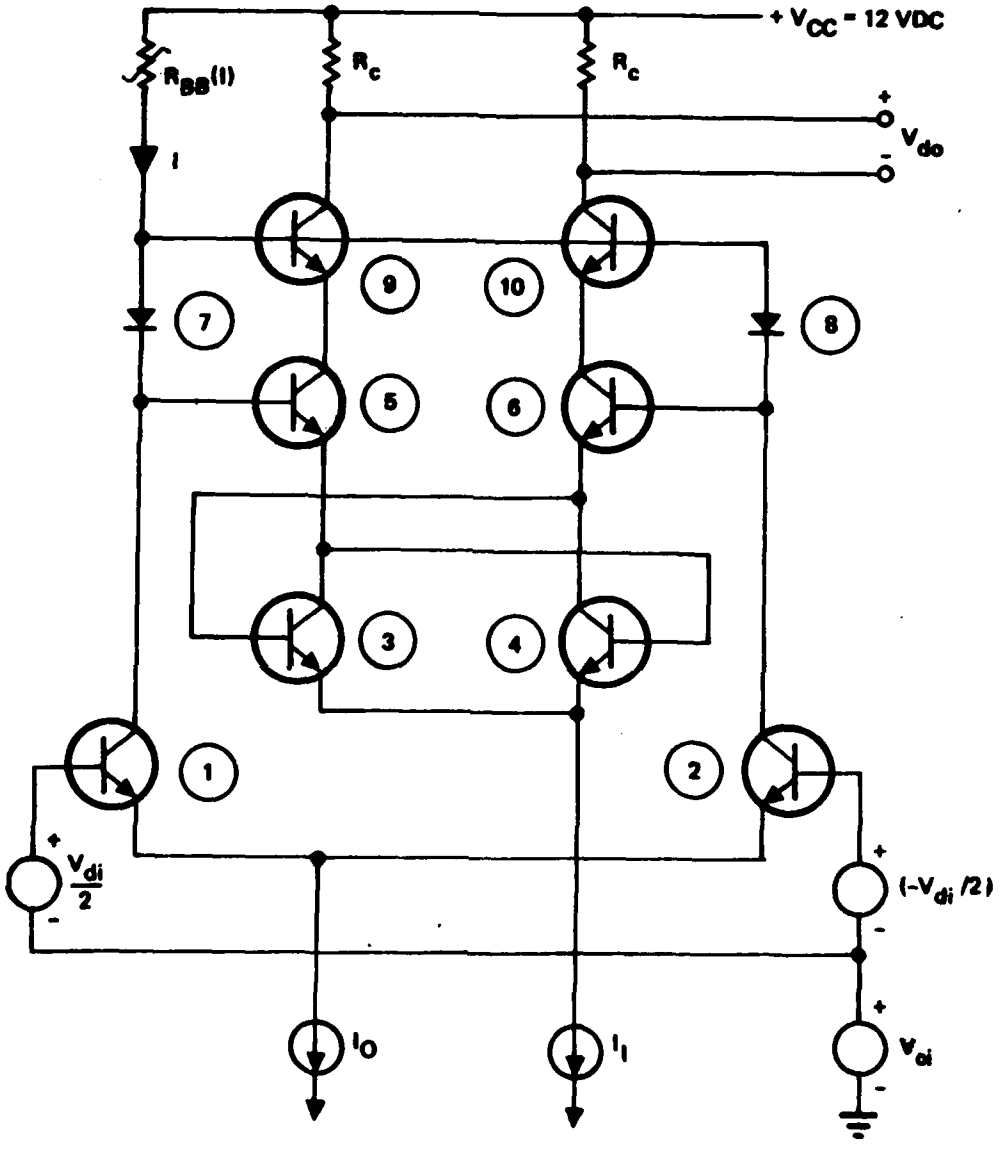


Figure (4.11). Basic Negative Resistance Gain Cell.

output voltage is V_{do}. High gain is established as a direct consequence of transistors 5 and 6 by the regenerative circuit comprised of transistors 3 and 4.

4.4.1 Differential Gain

The differential voltage gain, $A_{dm} = V_{do}/V_{di}$, may be ascertained through analysis of the differential mode half circuit given in figure (4.12). In the interest of analytical simplicity, the output resistances of all transistors are assumed to be infinitely large, and all series collector resistances are taken to be zero. Parameters r_{Bj}, r_{ej}, $r_{\pi j}$, and g_{mj} respectively symbolize dynamic base resistance, series emitter resistance, base-emitter junction diffusion resistance, and forward transconductance of the jth transistor. Resistance R_{D7} is used to model the small signal terminal characteristics of the diode defined as device #7 in figure (4.11). Since this device is a transistor whose base and collector terminals are short-circuited, its incremental model is as depicted in figure (4.13). With the help of this model, it is a straightforward task to show that

$$R_{D7} = \frac{V}{i} = r_{e7} + \frac{r_{B7} + r_{\pi 7}}{\beta_7 + 1}, \tag{4-38}$$

where in this and ensuing calculations,

$$\beta_j \triangleq g_{mj} r_{\pi j}. \tag{4-39}$$

The resistance, $(-R_{EQ})$, at terminal E5', which is the intrinsic emitter node of device #5, is one-half of the net differential resistance seen between the intrinsic emitters of devices #5 and #6. As inferred by the symbology, this resistance is negative, and this fact can be confirmed by investigating the differential resistance seen looking into the collectors of devices #3 and #4. The pertinent small signal

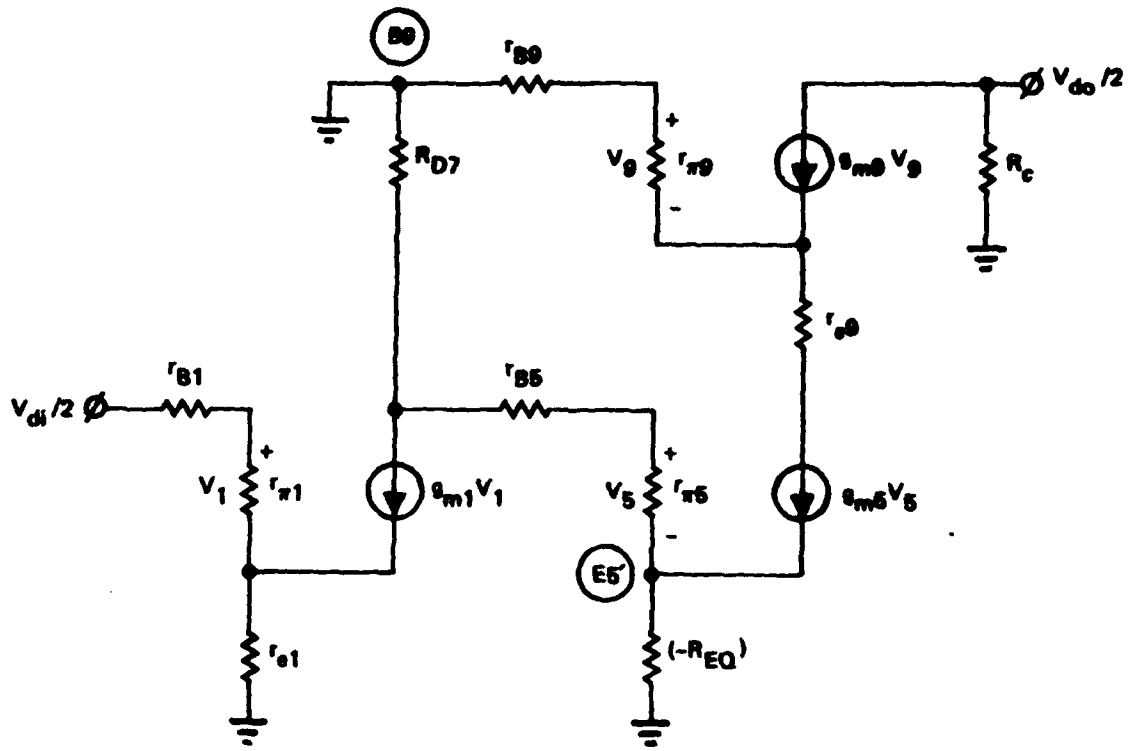


Figure (4.12). Differential Mode Half Circuit Small-Signal Model of Basic Gain Cell. Note that node B9 is grounded since no differential voltage can appear across the bases of transistors #9 and #10.

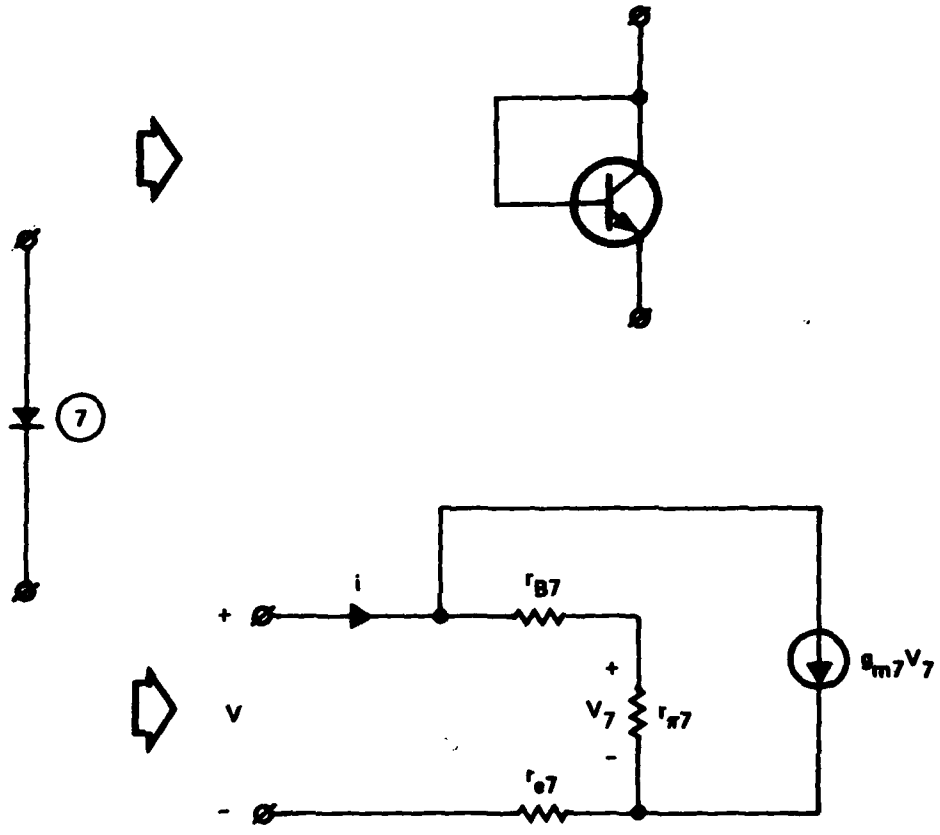


Figure (4.13). Incremental Model of Diode-Connected Transistor (Device #7).

model, assuming that transistors #3 and #4 are matched, is offered in figure (4.14). It can be shown that the differential resistance in question is

$$R_{dc} = \frac{V_c}{i_c} = \frac{2[r_{B3} + r_{\pi 3} + (\beta_3 + 1)r_{e3}]}{1 - \beta_3}, \qquad (4\text{-}40)$$

which is clearly negative for practical values of β_3. It follows that for the half circuit model,

$$-R_{EQ} = -\left\{\frac{r_{B3} + r_{\pi 3} + 2r_{e3}}{\beta_3 - 1}\right\}. \qquad (4\text{-}41)$$

Observe that $(-R_{EQ}) < 0$ for $\beta_3 > 1$.

An analysis of the complete model offered in figure (4.12) shows that the differential mode gain is given by

$$A_{dm} = \frac{V_{do}}{V_{di}} = \left\{\frac{\beta_1 R_c}{r_{B1} + r_{\pi 1} + (\beta_1 + 1)r_{e1}}\right\}\left\{\frac{\beta_5 R_{D7}}{R_{D7} + r_{B5} + r_{\pi 5} - (\beta_5 + 1)R_{EQ}}\right\}, \qquad (4\text{-}42)$$

where β_9 is presumed much larger than unity. Clearly, the gain can be rendered boundless by constraining the denominator in the second factor on the right-hand side to zero. In practice, it is doubtful that such a constraint can be implemented precisely owing to uncertainties in device parameter values. Moreover, it must be remembered that (4-42) is predicated on approximations which by and large render (4-42) as an upper limit on the practical differential gain that can be attained. For example, the effect of finite output resistance is to degrade gain so that even if the denominator factor in question is set to zero, the gain magnitude actually realized remains finite.

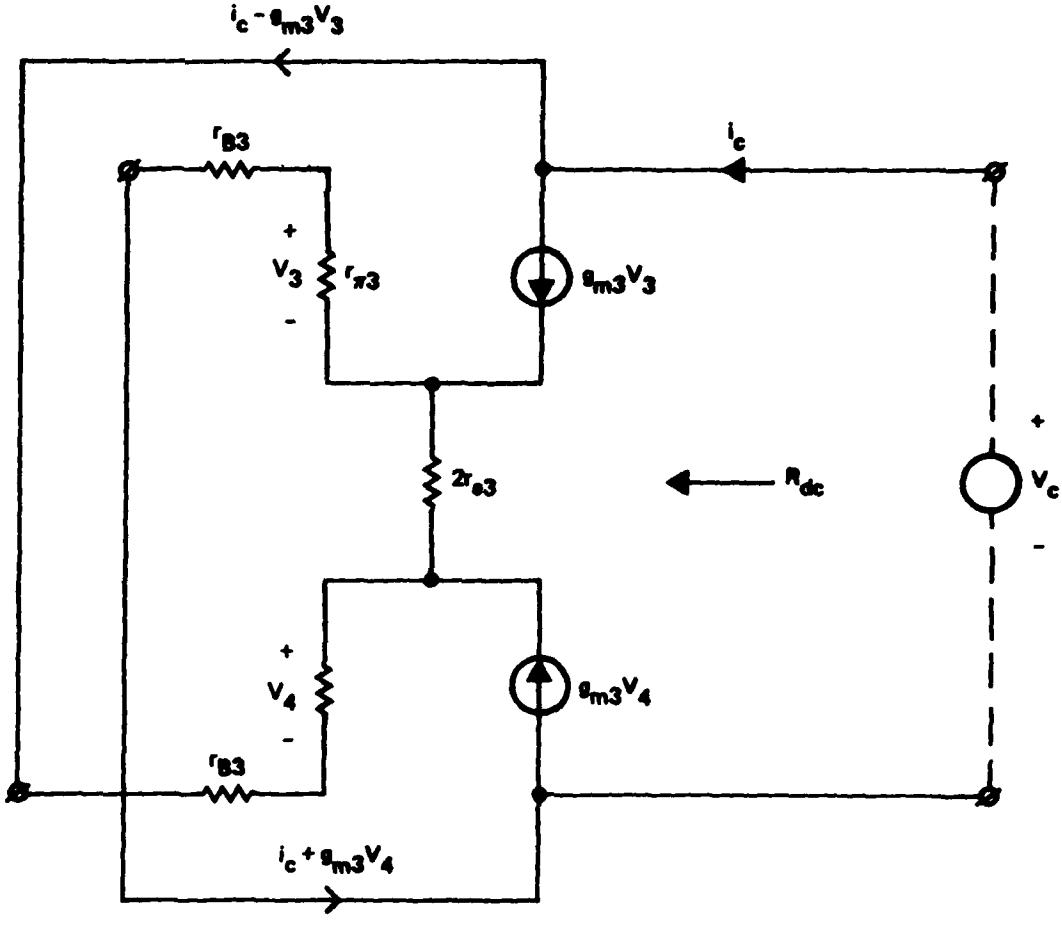


Figure (4.14). Differential Model of Subcircuit Composed of Devices #3 and #4.

It is also crucial to note that stable operation of the circuit in figure (4.11) necessarily implies zero low frequency phase shift. To underscore the significance of this point, let

$$R_{D7} + r_{B5} + r_{\pi 5} \triangleq K(\beta_5 + 1)R_{EQ}, \tag{4-43}$$

where K is a designable constant. Then for $\beta_5 >> 1$, (4-42) reduces to

$$A_{dm} = \left\{\frac{\beta_1 R_c}{r_{B1} + r_{\pi 1} + (\beta_1 + 1)r_{e1}}\right\}\left\{\frac{R_{D7}}{(K - 1)R_{EQ}}\right\}. \tag{4-44}$$

It is now clear that the uncertainty inherent in precise maintenance of K = 1, coupled with the requirement of zero phase shift at low frequencies, demands

$$K > 1. \tag{4-45}$$

Of course, a very large gain constrains K to be near unity.

4.4.2 Design Considerations

Assuming that transistors #5 and #3 are identical, (4-43) and (4-41) combine to yield

$$R_{D7} = 2Kr_{e5} + \left\{K - 1 + \frac{K + 1}{\beta_5}\right\}(r_{B5} + r_{\pi 5}), \tag{4-46}$$

assuming $\beta_5 >> 1$. It should be noted that (4-46) implies a ratio constraint between I_0 and I_I. For example, assume r_{e5} = 5 ohms, β_5 = 50, r_{b5} = 250 ohms, K = 1, and let the collector current through transistor #5 be 600 μA. Then, since

$$r_{\pi 5} = \frac{\beta_5 V_T}{I_{c5}} = 2156 \text{ ohms}$$

at 27°C, the required value of R_{D7} is 106.24 ohms. Assuming further that transistor #7 is identical to transistor #5, (4-38) provides

$$r_{\pi 7} = 4913 \text{ ohms},$$

which corresponds to

$$I_{C7} = \frac{\beta_7 V_T}{r_{\pi 7}} = 263.3 \ \mu A.$$

In order to ensure no phase reversal at low frequencies, I_{C7} is hereby chosen to be 250 μA, and thus

$$R_{D7} = 111.4 \text{ ohms},$$

whence by (4-46)

$$K = 1.0021.$$

The foregoing computations imply

$$\left.\begin{aligned} I_O &= 500 \ \mu A \\ I_I &= 1.2 \text{ mA} \end{aligned}\right\}. \qquad (4\text{-}47)$$

Using (4-41),

$$R_{EQ} = \frac{250 + 2156 + 10}{49} = 49.306 \text{ ohms}.$$

Noting that the collector currents of devices #1 and #7 are virtually identical, (4-44) resultantly predicts

$$A_{dm} = 9.929 R_C.$$

For a differential mode gain of 12,000 (81.6 dB), R_c = 1208 ohms. To allow for various attenuations incurred by model elements that are ignored in this analysis, choose

$$R_c \geq 1500 \text{ ohms.} \tag{4-48}$$

The maximum swing in the differential output voltage, V_{do} is

$$\Delta V_{do} \approx 2I_I R_c; \tag{4-49}$$

this is to say that the voltage excursion at the collector of either transistor #9 or #10 is from a voltage of $(V_{CC} - I_I R_c)$-to-V_{CC}. Thus, for $R_c \geq 1500$ ohms and $I_I \approx 1.2$ mA, $\Delta V_{dc} \geq 3.6$ volts. Obviously, this swing is attainable if and only if transistors #9 and #10 are never allowed to saturate. Saturation of these devices is precluded by biasing the bases of #9 and #10 at a voltage which is less than $(V_{CC} - I_I R_c) = 10.2$ volts. A bias level of 8.7 volts is chosen, and as a result, the bases of transistors #5 and #6 rest at approximately 7.9 volts. To ensure optimal linear operation of input transistors #1 and #2, a common mode quiescent input voltage of 4.7 volts is chosen.

4.5 Multiple Transistor Current Sources

When utilized as a current sink in the tail circuit of an emitter coupled pair, an active current source is conducive to excellent common mode rejection characteristics at low-to-moderate frequencies. At progressively higher frequencies, common mode performance deteriorates, owing to the capacitive nature of the driving point impedance associated with the collector of an npn current source. Despite the last fact, current sources are useful in numerous OAT RFLSI applications, particularly if the highest signal frequency of interest is less than 10% of device f_T. Moreover, it is possible to exploit the omnipresent capacitance of current source output impedance for the purpose of broadbanding a frequency neutralized differential pair.

4.5.1 Current Mirror

In the circuit of figure (4.15), transistors Q1 and Q2 are identical and since both base emitter voltages are the same, both transistor base currents are identical; i.e., the base currents are "mirrored."

From figure (4.15), the output current of the source is easily shown to be

$$I_K = \frac{h_{FE2}(V_I - V_{BE})}{(h_{FE1} + 2)R} . \tag{4-50}$$

Static current gain parameters, h_{FE2} and h_{FE1} are not equal, despite identical transistors, because the collector base bias of Q1 differs from that of Q2. If the Early voltage [15] of each device is V_{CR},

$$h_{FE2} \approx \beta_o \left\{ 1 + \frac{V_{CE2} - V_{BE}}{V_{CR}} \right\}, \tag{4-51}$$

while

$$h_{FE1} \approx \beta_o, \tag{4-52}$$

where β_o is the common emitter short circuit static current transfer ratio under the condition of zero bias across the collector-base junction. Nevertheless, note that for $h_{FE1} >> 2$, excellent thermal characteristics are obtained if (1) the thermal characteristics of h_{FE2} track with those of h_{FE1}, and (2) the reference voltage, V_I, is designed to provide a thermal coefficient of nominally one forward-biased base-emitter junction voltage.

It can also be shown that the dynamic output resistance, say R_K, at low frequencies is

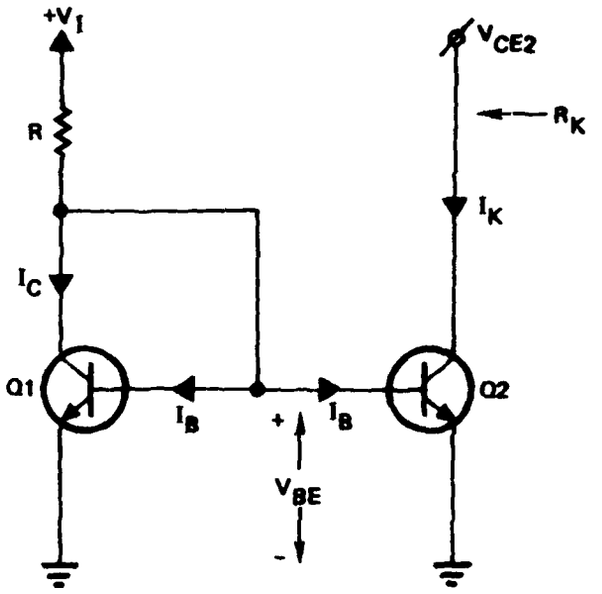


Figure (4.15). Simple Current Mirror

$$R_K = r_{cc} + \frac{F_E}{g_o}, \tag{4-53}$$

where r_{cc} is the net device resistance in series with the collector, g_o is the small-signal output conductance, and

$$F_E = 1 + (g_m + g_o)r_e. \tag{4-54}$$

In (4-54), g_m represents forward transconductance, and r_e symbolizes the net intrinsic resistance in series with the emitter.

4.5.2 Two-Transistor Mirror

The current source of figure (4.15) requires $\beta_o >> 2$ to obtain nominal performance insensitivity with respect to current gain. For low beta devices, the source shown in figure (4.16) proves valuable. For this circuit,

$$I_K = \left(\frac{h_{FE2}}{h_{FE1} + \frac{2}{h_{FE3} + 1}}\right)\left(\frac{V_I - V_{BE}}{R}\right), \tag{4-55}$$

while the expression for R_K remains as per (4-53). Note that the desired insensitivity with respect to current gain is now achieved if $h_{FE1}(h_{FE3} + 1) >> 2$.

4.5.3 Widlar Source [16]

Enhanced design flexibility is afforded by the current source of figure (4.17). For $R_1 = 0$, the circuit becomes known as the Widlar current source, which is capable of very small I_K without the need for abnormally large resistors or grossly mismatched areas for Q1 and Q2.

From figure (4.17),

$$V_{BE1} + (h_{FE1} + 1)I_{B1}R_1 = V_{BE2} + (h_{FE2} + 1)I_{B2}R_2.$$

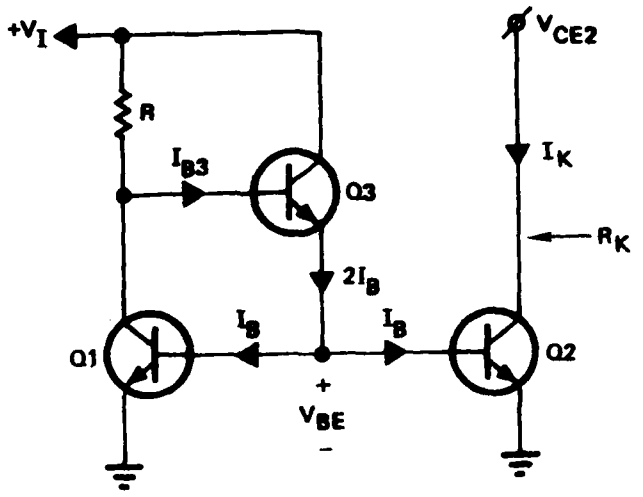


Figure (4.16). Two-Transistor Mirror.

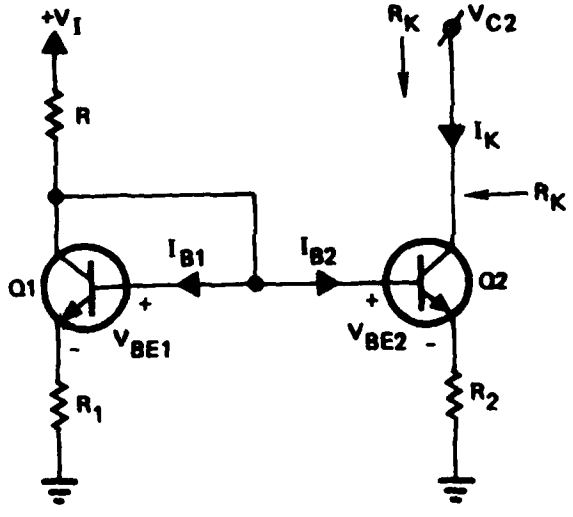


Figure (4.17). Widlar Current Source.

Recalling the classical Ebers-Moll model [17],

$$V_{BE1} \approx V_T LN \frac{I_{B1}\beta_{01}}{I_{S1}}$$

and

$$V_{BE2} = V_T LN \frac{I_{B2}\beta_{02}}{I_{S2}} ,$$

$$V_{BE1} - V_{BE2} = V_T LN \left(\frac{I_{B1}}{I_{B2}}\right)\left(\frac{I_{S2}}{I_{S1}}\right)\left(\frac{\beta_{01}}{\beta_{02}}\right)$$

$$= V_T LN M_B \left(\frac{I_{B1}}{I_{B2}}\right),$$

where

$$M_B = \left(\frac{I_{S2}}{I_{S1}}\right)\left(\frac{\beta_{01}}{\beta_{02}}\right)$$

is unity for matched devices. It follows that

$$\frac{V_T}{I_{B1}} LN\left(M_B \frac{I_{B1}}{I_{B2}}\right) + (h_{FE1} + 1)R_1 = (h_{FE2} + 1)R_2 \frac{I_{B2}}{I_{B1}} .$$

More usefully,

$$\frac{I_K}{I_{C1}} = \left(\frac{\alpha_2}{\alpha_1}\right)\left(\frac{R_1}{R_2}\right) + \frac{V_T\alpha_2}{R_2 I_{C1}} LN\left\{\left(\frac{I_{S2}}{I_{S1}}\right)\left(1 + \frac{V_{CE2} - V_{BE2}}{V_{CR}}\right)\frac{I_{C1}}{I_K}\right\} \quad (4\text{-}56)$$

where

$$\left.\begin{aligned} \alpha_2 &= \frac{h_{FE2}}{h_{FE2}+1} \\ \alpha_1 &= \frac{h_{FE1}}{h_{FE1}+1} \\ h_{FE1} &= \beta_{01} \quad \text{(ignoring series device resistances)} \\ h_{FE2} &\approx \beta_{02}\left\{1+\frac{V_{CE2}-V_{BE2}}{V_{CR}}\right\} \end{aligned}\right\} \qquad (4\text{-}57)$$

For a prescribed ratio, I_K/I_{C1}, (4-56) fixes I_{C1}, whence

$$V_I = R\left\{\frac{I_{C1}}{h_{FE1}}+\frac{I_K}{h_{FE2}}+I_{C1}\right\}+V_{BE1}+R_1\left\{\frac{I_{C1}}{h_{FE1}}+I_{C1}\right\}$$

or

$$V_I = V_{BE1}+I_{C1}\left\{\frac{R_1+R}{\alpha_1}+\frac{R}{h_{FE2}}\left(\frac{I_K}{I_{C1}}\right)\right\} \qquad (4\text{-}58)$$

For matched devices, $I_{S2} = I_{S1}$. Then if I_{C1} and I_K are of the same order of magnitude, the natural logarithmic term is insignificant, particularly if the Early voltage is large. Accordingly, (4-56) shows that

$$\frac{I_K}{I_{C1}} \approx \frac{R_1}{R_2} \quad (\text{since } \alpha_2/\alpha_1 \approx 1)$$

and

$$V_I \approx V_{BE1}+I_{C1}\left\{\frac{R_1+R}{\alpha_1}+\left(\frac{R}{h_{FE2}}\right)\left(\frac{R_1}{R_2}\right)\right\}.$$

Notice that the devices need not be perfectly matched since the current ratio, I_K/I_{C1} is dependent on the natural logarithm of an area mismatch.

The evaluation of dynamic output resistance, R_K, is considerably simplified if the net base and collector resistances are ignored for each transistor. The pertinent simplified model appears in figure (4.18a). Since the base and collector of Q1 is shorted, the $g_{m1}V_{A1}$ generator is equivalent to a conductance, g_{m1}. Thus, the net resistance in parallel with R_2 is

$$R_p = \frac{1}{g_{B2}} + R \| \left\{ R_1 + \frac{1}{g_{m1} + g_{01} + g_{B1}} \right\}. \tag{4-59}$$

Since g_{m1} is large,

$$R_p \approx \frac{1}{g_{B2}} + R \| R_1 = \frac{1 + g_{B2}(R \| R_1)}{g_{B2}}. \tag{4-60}$$

The model resultantly reduces to the topology of figure (4.18b).

After considerable manipulation, the desired expression for R_K evolves as

$$R_K \approx \left[\frac{V_{CR} + V_{BE2} - V_{CE2}}{I_K} \right] \left[1 + \frac{h_{FE2} R_2}{R_2 + R_p} \right]. \tag{4-61}$$

Observe that the output resistance is maximal if $R_2 >> R_p$. Unfortunately, this constraint is difficult to satisfy in practice. Additionally, note that the resistance is inversely proportional to the quiescent current, I_K, flowing in the collector of transistor Q2 in figure (4.17).

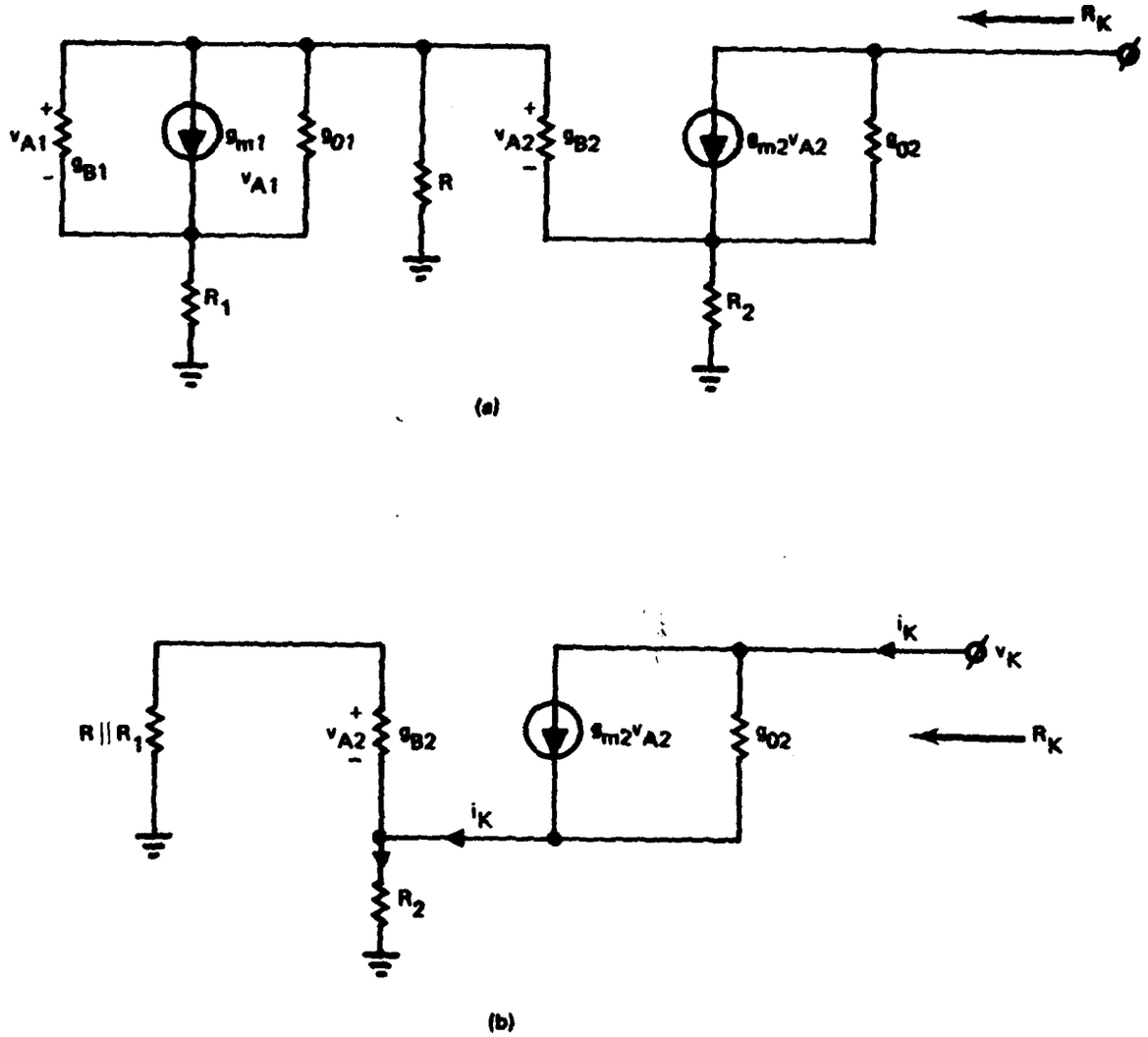


Figure (4.18). (a) Small-Signal Equivalent Circuit of Widlar Current Source.

(b) Reduced Small-Signal Model.

4.5.4 Cascode Source

The easiest way of achieving $R_2 >> R_p$ in (4-61) is to supplant R_2 in figure (4.17) by yet another bipolar device which serves to act as a current source in itself. The resultant configuration becomes as drawn in figure (4.19) and is known as a cascode-compensated current source. The dynamic output resistance is

$$R_K = \left(\frac{V_{CR} + V_{BE2} - V_{CE2}}{I_K}\right)(h_{FE2} + 1), \qquad (4\text{-}62)$$

which, as might be expected, reflects the resistance value predicted by (4-61) with R_2 set to a resistance that is substantially larger than R_p.

Since transistors Q3 and Q4 are forced to support nominally identical collector-base biases, the static current transfer ratio for these devices is taken to be the same; that is, $h_{FE3} = h_{FE4} = h_{FE}$. Then, the static output current can be shown to be

$$I_K = \left(\frac{h_{FE2}}{h_{FE2} + 1}\right)\left[\frac{h_{FE}}{2 + h_{FE}\,1 + \frac{1}{h_{FE2} + 1}}\right]\left[\frac{V_I - V_{BE1} - V_{BE3}}{R}\right]. \qquad (4\text{-}63)$$

For $h_{FE2} >> 1$ and $h_{FE} >> 1$, (4-63) reduces to

$$I_K \approx \frac{V_I - V_{BE1} - V_{BE3}}{R}. \qquad (4\text{-}64)$$

Both of these results show that if I_K is to be rendered thermally stable, the reference supply must possess a thermal coefficient that mirrors the thermoelectrical properties of a series connection of two forward biased base-emitter junctions.

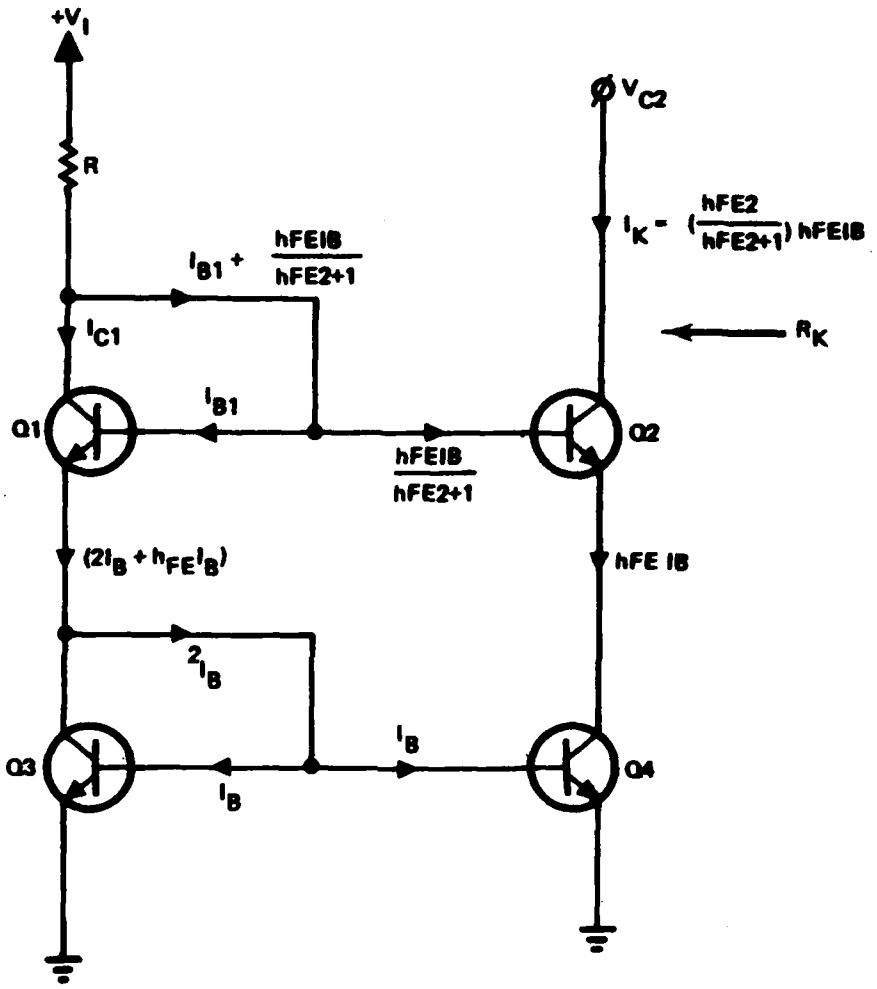


Figure (4.19). Cascode Current Source Which Yields Very High Output Resistance.

4.5.5 Wilson Source

The Wilson source configured in figure (4.20) is yet another high output resistance configuration. Its prime advantage over the cascode configuration is that it uses one less transistor. Since the base-collector drops of Q1 and Q3 are only one forward biased junction voltage apart, the current gains of these transistors can be presumed identical. Thus, for identical transistors, it materializes that

$$I_K = \left(\frac{h_{FE2}}{h_{FE2}+1}\right)\left\{\frac{(V_I - V_{BE1} - V_{BE2})/R}{\frac{h_{FE}}{h_{FE}+2} + \frac{1}{h_{FE2}+1}}\right\}. \qquad (4\text{-}65)$$

Observe that when V_{C2} changes due, for example, to common mode signal excitation in a differential pair, most of the voltage changes are absorbed by Q2. This situation reflects the fact that the collector-emitter voltage of Q3 is the base-emitter voltage of Q3 and therefore, the collector-emitter port of Q3 features low resistance. As a result, I_B is relatively constant, and the source displays high output resistance.

4.5.6 Common Mode Rejection Revisited

The foregoing considerations and analyses can be prudently applied to the problem of optimizing the high frequency common mode response of the simple differential pair depicted in figure (4.21a). In particular, let Thevenin signal sources $v_{s1}(s)$ and $v_{s2}(s)$ possess a transformed common mode input signal component, $v_{ci}(s)$. The possibility of determining an optimal tail termination, modeled in figure (4.21a) by the Norton circuit consisting of I_I in shunt with impedance $Z_k(s)$, is to be investigated.

The pertinent equivalent circuit is offered in figure (4.21b). Short circuit common emitter admittance parameters are used in the half circuit model in order to encumber all pertinent high frequency input, output, feedback, and feed-forward effects. These parameters can be expected to be complex functions of frequency.

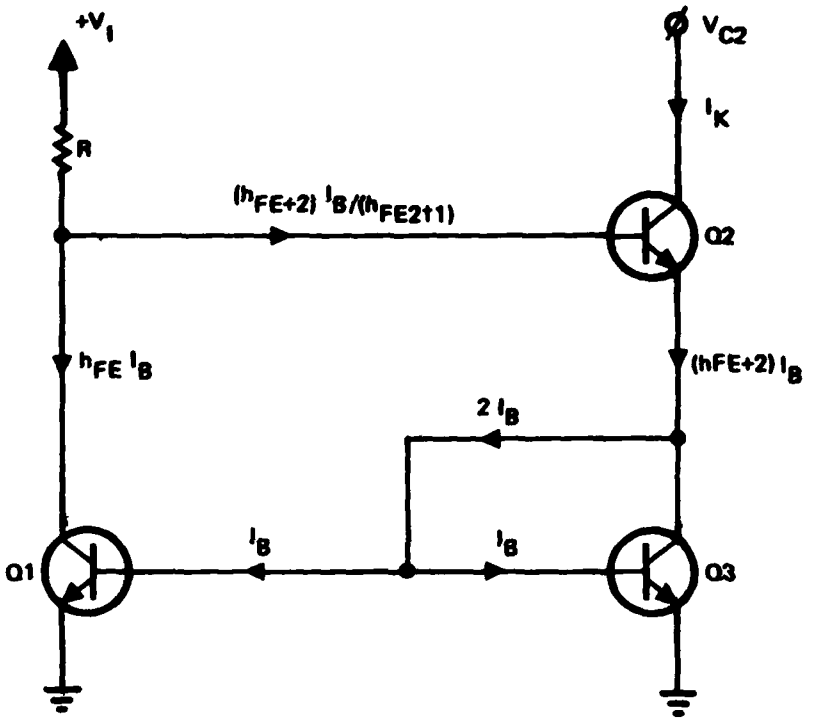


Figure (4.20). Wilson Alternative to Cascode Current Source.

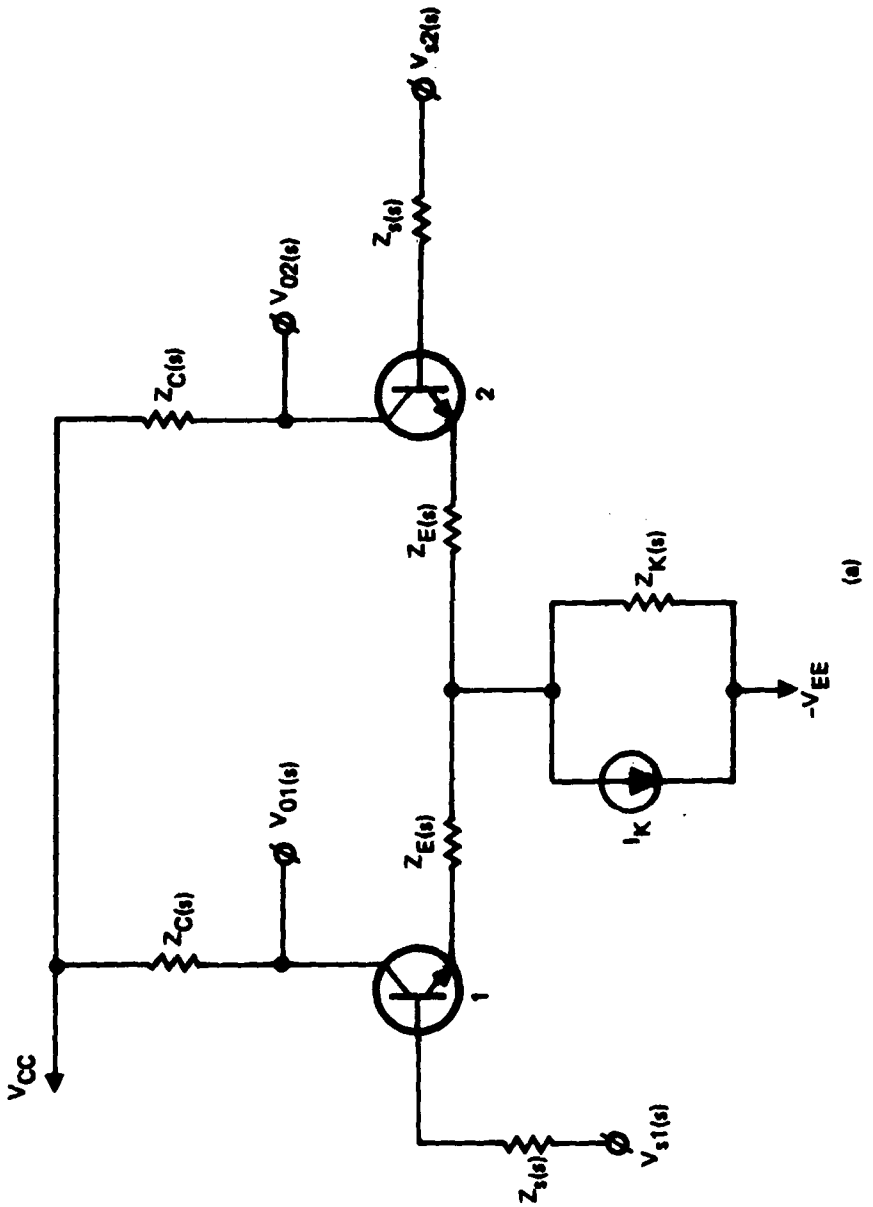


Figure (4.21). (a) AC Schematic Diagram of Simple Differential Pair.

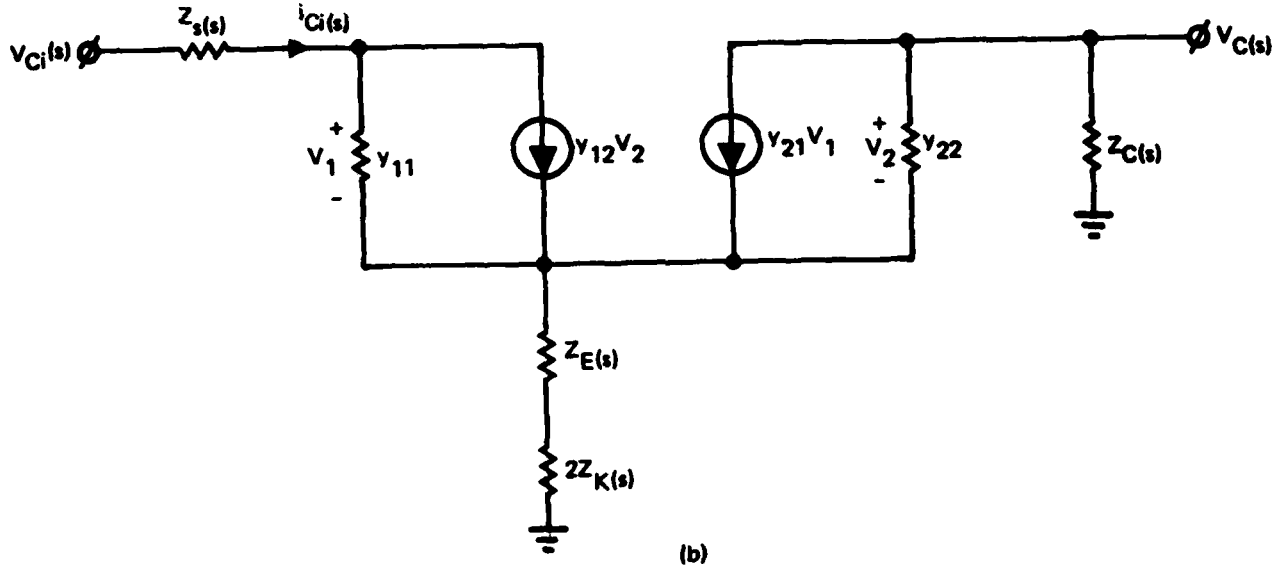


Figure (4.21) (b) Small-Signal, y-Parameter Half Circuit Model for Investigation of Common Mode Response.

If "optimal" is taken as enforcement of a constraint of zero output common mode signal, a constraint of zero output common mode signal, then $v_c(s)$ in figure (4.21b) is zero. Accordingly,

$$y_{21}v_1 + y_{22}v_2 = 0.$$

From figure (4.21b),

$$v_c(s) = v_2 + \{Z_E(s) + 2Z_K(s)\}\{y_{11}v_1 + y_{12}v_2\}$$

$$= v_2\left\{1 + [Z_E(s) + 2Z_K(s)]\left[y_{12} - \frac{y_{11}y_{22}}{y_{21}}\right]\right\}.$$

It follows that

$$Z_E(s) + 2Z_K(s) = \frac{y_{21}}{y_{11}y_{22} - y_{12}y_{21}}. \qquad (4\text{-}66)$$

Equivalently,

$$Z_E(s) + 2Z_k(s) = \frac{h_{fe}(s)}{y_{22} - h_{fe}(s)y_{12}}, \qquad (4\text{-}67)$$

where $h_{fe}(s) = y_{21}/y_{11}$ is the small-signal common emitter short circuit current gain. Interestingly enough, (4-66) and (4-67) show that the tail impedance commensurate with an ideal common mode response characteristic is not infinitely large, unless the transistors conform to the idealized constraint, $y_{22} = y_{12} = 0$.

Assume now that the transistors in the differential pair are frequency neutralized [18], [19]. Then (4-67) becomes

$$Z_E(s) + 2Z_K(s) \approx \frac{h_{fe}}{y_{22A}} . \qquad (4\text{-}68)$$

One may reason that the right-hand side is roughly the impedance seen at the output of the cascode current source of figure (4.19) or even the simple source of figure (4.16). For $|Z_E(s)| << |2Z_K(s)|$, which may require a small capacitive shunt across resistor R_E in order that low frequency performance attributes not be perturbed, (4-68) gives

$$Z_K(s) \approx \frac{h_{fe}}{2y_{22A}} . \qquad (4\text{-}69)$$

At low frequencies, $y_{22A} \approx g_o$, which is directly proportional to current. To the extent that y_{22A} remains current proportional at all frequencies, $2y_{22A}$ is the short circuit output admittance of the current source, which carries nominally twice the current of each active device in the neutralized differential pair. Unfortunately, the assumption that both real and imaginary parts of y_{22A} are current proportional is weak. The implication, of course, is that the common mode gain can never be made precisely equal to zero, but rejection ratios in excess of 50 dB are attainable through judicious invocation of the foregoing design guidelines.

Figure (4.22) depicts a plausible basic topology for a differential pair that is optimized in the sense of maximal common mode rejection ratio. The circuit utilizes the cascoded current source of figure (4.19) for the emitter coupled tail termination. It is excited by the voltage reference discussed in section (4.1) and, in accordance with (4-63), this reference is designed to supply a thermal coefficient that is nominally equivalent to that of the voltage developed across the series interconnection of two forward biased base-emitter junction diodes. The differential pair is frequency neutralized by transistors QC1 and QC2.

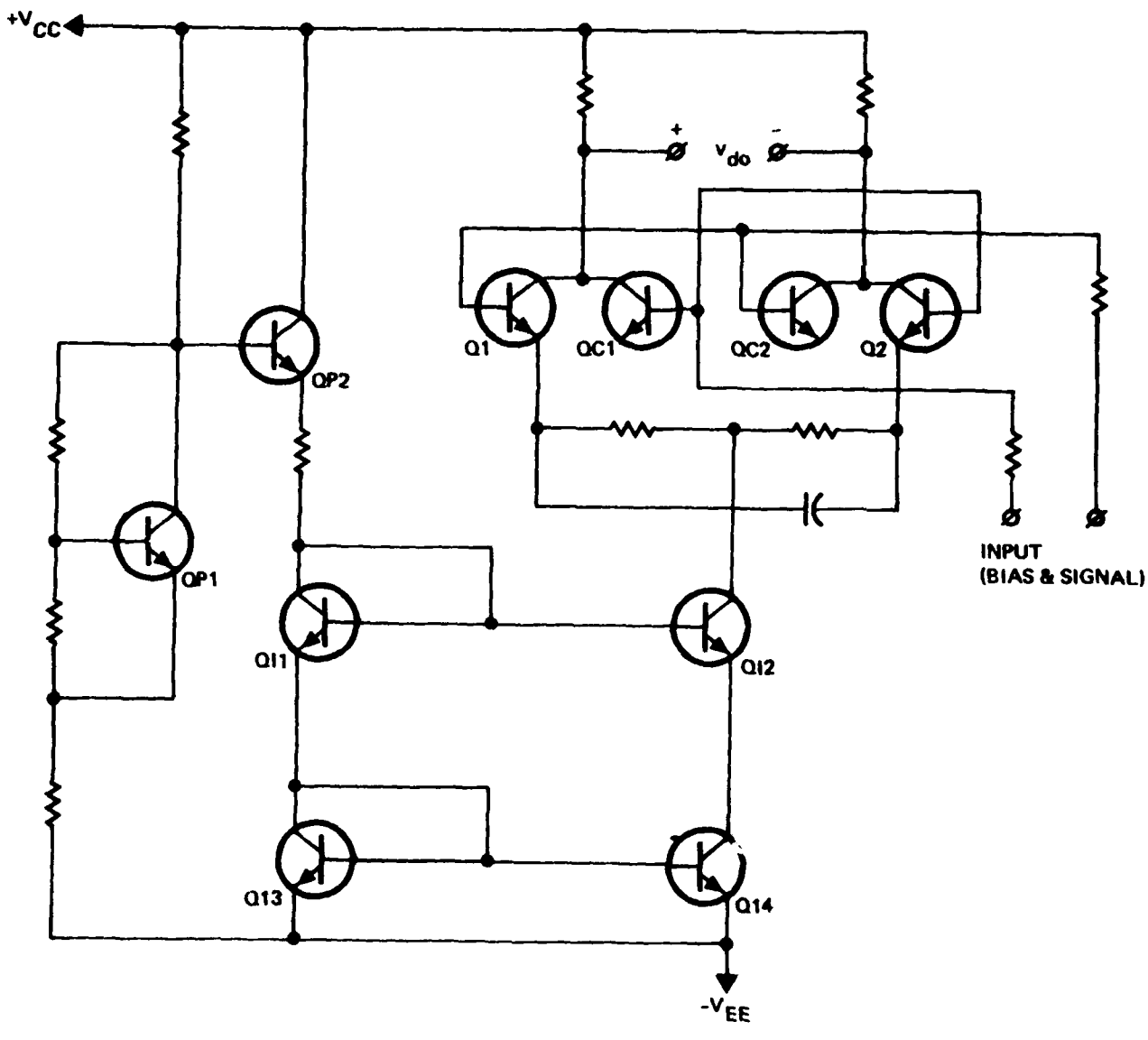


Figure (4.22). Neutralized Differential Amplifier With Common Mode Compensation.

5.0 CIRCUIT SET 1 (RFCS-1)

Circuit Set 1, which is symbolically referred to as RFCS-1, is a chip that contains eight (8) RFLSI building block candidates, seven (7) test transistors, and three (3) test inductors. The fabricated RFLSI circuits are an RF amplifier, an IF amplifier, an analog multiplier, an operational amplifier, three voltage controlled oscillators, and an RF switch. Figure (5.1) pictorially displays RFCS-1 layout.

5.1 RF Amplifier

The RF amplifier utilizes active matching to achieve power gain at L-band frequencies. Active matching has numerous advantages over such other broadbanding techniques as feedback, compounding of gain devices, neutralization, and passive matching. Feedback seems viable in the sense of stability only for frequencies below 1 GHz with the current OAT process. Compound gain devices and neutralization are useful approaches to the design of only IF amplifiers. Passive spiral inductor amplifiers consume large chip area and are unacceptably sensitive to critical transistor parameters.

The only specification for this amplifier is that it provide as much gain as possible at 1.6 GHz, while keeping power consumption at a reasonable level. To ensure against parasitic oscillations, the amplifier is completely differential. A single-ended input can be accommodated by grounding the complimentary side of the input differential pair at the ground terminal of the transmission line supplying that input.

5.1.1 Circuit Definition

The circuit, shown schematically in figure (5.2), consists of three common-emitter differential amplifier stages (Q_6-Q_7, Q_{12}-Q_{13}, Q_{18}-Q_{19}) with active interstage matching networks. These networks consist of a transistor in an inverted common-collector configuration (Q_4, Q_5, Q_{10}, Q_{11}, Q_{16}, Q_{17}), which exhibits inductive output impedance, an emitter follower (Q_8, Q_9, Q_{14}, Q_{15}), and a capacitor (C_7-C_{10}).

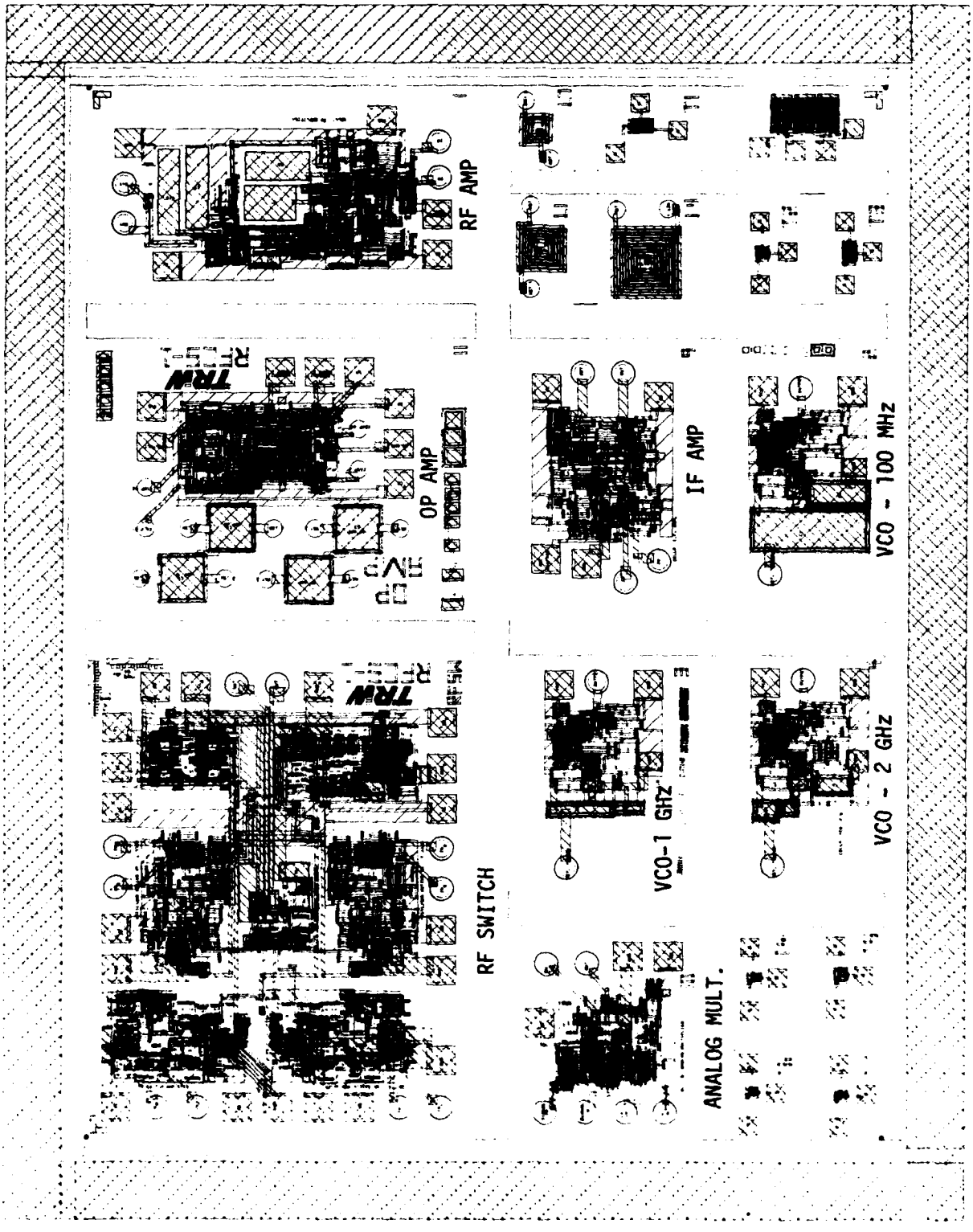
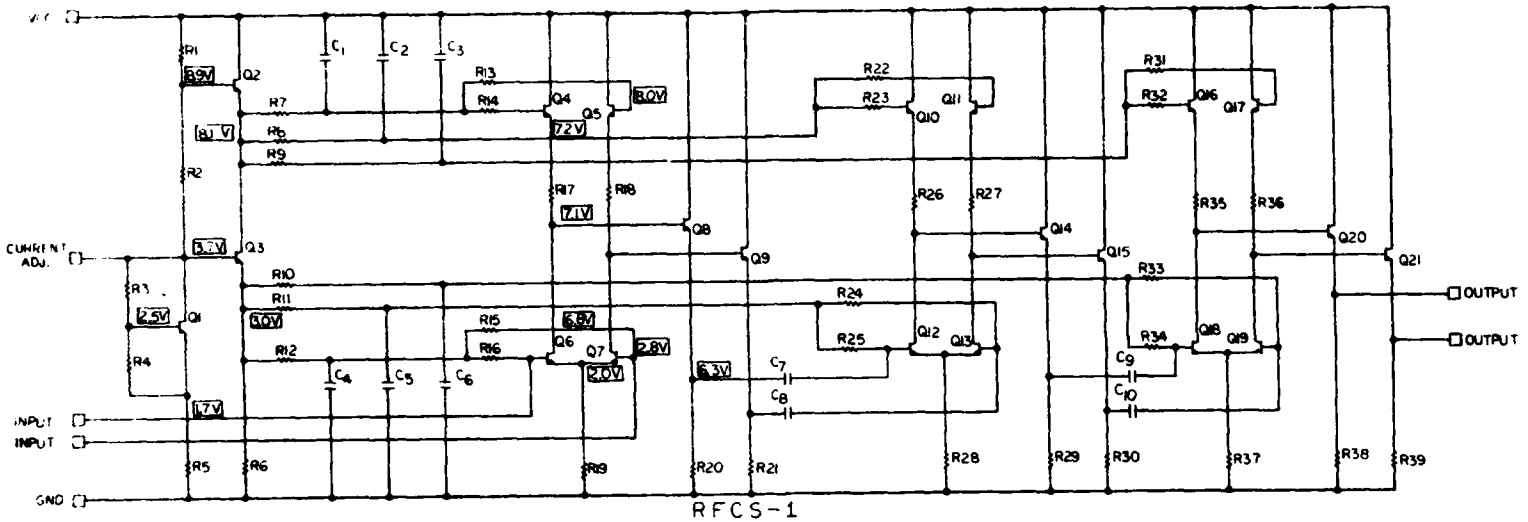


Figure (5.1). Layout of RFCS-1.



RFCS-1
RF AMPLIFIER

①

RESISTOR VALUES ARE IN OHMS AT 200 OPS

1. R1=2.1K
2. R2=36K
3. R3=1.7K
4. R4=1.4K
5. R5=1.1K
6. R6=4.7K
7. R7,R8,R9,R10,R11,R12=2K
8. R13,R14,R22,R23,R31,R32=350
9. R15,R16,R24,R25,R33,R34=1K
10. R17,R18,R26,R27,R35,R36=50
11. R19,R28,R37=500
12. R20,R21,R29,R30,R38,R39=31K
13. C1-C6=30pf
14. C7-C10=15pf

NOTES:
1. VCC=+12V
2. ALL TRANSISTORS ARE 2T2L12W3
3. C1-C6 ARE BURIED LAYER TO ISOLATION DIODES.
4. INPUT AND OUTPUT PADS ARE 4MILS IN DIAMETER.
5. P_D = 320mw

APPROVED
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22 May 1979

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Figure (5.2). Schematic Diagram of RF Amplifier

Transistors Q_1-Q_3 provide temperature invariant bias to each gain stage. Capacitors C_1-C_6 and resistors R_7-R_{12} form low-pass filters which decouple the bias circuitry from the gain stages. Power consumption is 320 mW.

5.1.2 Circuit Analysis and Design

As mentioned previously, the RF amplifier exploits the output inductance of an inverted common-collector configuration (ICC) for gain peaking at L-band. Figure (5.3a) shows the ICC configuration, and the small-signal model used for the ICC analysis is depicted in figure (5.3b).

The output impedance, $Z_o(s)$, is given by [20]

$$Z_o(s) = \frac{V_T(s)}{I_T(s)} = R(s) + sL(s). \qquad (5\text{-}1)$$

In (5-1),

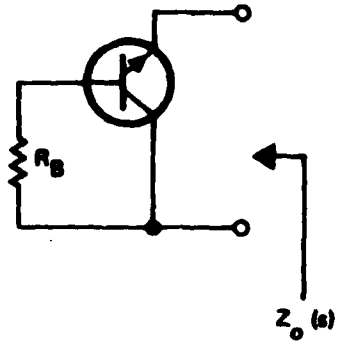
$$R(s) = \frac{r_\pi + R_{BB}\left(1 + \frac{s^2}{\omega_2\omega_\beta}\right)}{(\beta + 1)\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)} \qquad (5\text{-}2)$$

and

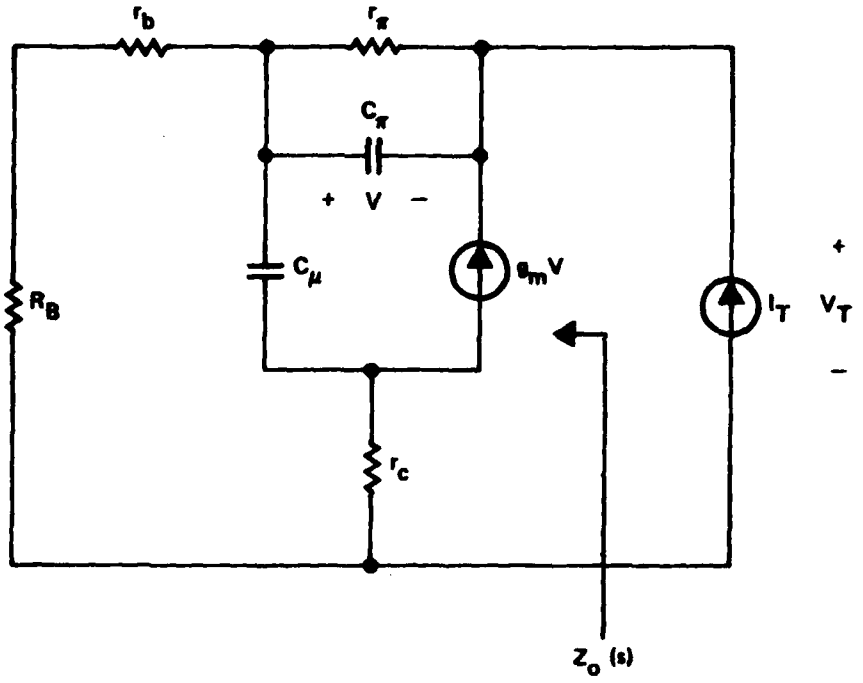
$$L(s) = \frac{\left(\frac{1}{\omega_2} + \frac{1}{\omega_\beta}\right)R_{BB} + \frac{r_\pi}{\omega_1}\left(1 + \frac{g_m r_c R_{BB}}{r_c + R_{BB}}\right)}{(\beta + 1)\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_T}\right)} \qquad (5\text{-}3)$$

where

$$R_{BB} = r_b + R_B, \qquad (5\text{-}4)$$



(a)



(b)

Figure (5.3). (a). Inverted Common Collector (ICC) Circuit.

(b). Small-Signal Model of (a).

$$\omega_\beta = \frac{1}{r_\pi C_\pi} , \tag{5-5}$$

$$\omega_T = \frac{g_m}{(C_\pi + C_\mu)} , \tag{5-6}$$

$$\omega_1 = \frac{1}{(R_{BB} + r_c)C_\mu} , \tag{5-7}$$

$$\omega_2 = \frac{1}{r_c C_\mu} , \tag{5-8}$$

$$\beta = g_m r_\pi \tag{5-9}$$

is the low frequency, short-circuit, common-emitter current gain of the transistor.

The expression for $Z_o(s)$ can be separated into real and imaginary parts, thereby yielding the output resistance, R_o, and output reactance, X_o, respectively:

$$R_o = \frac{\left[r_\pi + R_{BB}\left(1 - \frac{\omega^2}{\omega_2\omega_\beta}\right)\right]\left(1 - \frac{\omega^2}{\omega_1\omega_T}\right) + \omega^2\left(\frac{1}{\omega_1} + \frac{1}{\omega_T}\right)\left[R_{BB}\left(\frac{1}{\omega_2} + \frac{1}{\omega_\beta}\right) + \frac{r_\pi}{\omega_1}\left(1 + \frac{g_m g_c R_{BB}}{r_c + R_{BB}}\right)\right]}{(\beta + 1)\left[\left(1 - \frac{\omega^2}{\omega_1\omega_T}\right)^2 + \omega^2\left(\frac{1}{\omega_1} + \frac{1}{\omega_T}\right)^2\right]} \tag{5-10}$$

and

$$X_o = \frac{\omega\left[\left(\frac{1}{\omega_1} + \frac{1}{\omega_T}\right)\left(r_\pi + R_{BB}\left(1 - \frac{\omega^2}{\omega_2\omega_\beta}\right)\right) + \left(1 - \frac{\omega^2}{\omega_1\omega_T}\right)\left(R_{BB}\left(\frac{1}{\omega_2} + \frac{1}{\omega_\beta}\right) + \frac{r_\pi}{\omega_1}\left(1 + \frac{g_m r_c R_{BB}}{r_c + R_{BB}}\right)\right)\right]}{(\beta + 1)\left[\left(1 - \frac{\omega^2}{\omega_1\omega_T}\right)^2 + \omega^2\left(\frac{1}{\omega_1} + \frac{1}{\omega_T}\right)^2\right]} \tag{5-11}$$

Figure (5.4) uses (5-10) and (5-11) to display the dependence of output resistance, output reactance, and inductor Q on external base resistance at 1.6 GHz. The curves apply to an OAT 2T2L12W3 transistor, which has the following small-signal parameters:

$$\left.\begin{aligned} r_b &= 160\Omega \\ r_\pi &= 875\Omega \\ g_m &= .0693\mho \\ \beta &= 60.6 \\ C_\pi &= 1.94 \text{ pf} \\ C_\mu &= .216 \text{ pf} \\ r_c &= 60\Omega \end{aligned}\right\} . \qquad (5\text{-}12)$$

The signal path through one gain stage is defined in figure (5.5). The emitter follower-capacitor cascade provides both impedance matching between stages and ac coupling. There are three options in the gain path design; namely, transistor size, external base resistance of the ICC transistor, and the coupling capacitance. To compromise high frequency performance and power consumption, a 2T2L12W3 transistor (2 mA rating) is chosen.

The analysis of the gain path utilizes the sampled-parameter technique [21]. The amplifier power gain is optimized at only a single frequency (1.6 GHz), owing to the fact that the response is inherently broadband due to the low Q of the ICC inductor.

Figure (5.6) depicts the gain path of one amplifier stage as three cascaded two-ports. Two-port Y_γ models the output conductance of the active inductor as a parallel G-L network whose parameters depend on external base resistance. The composite y-parameters are

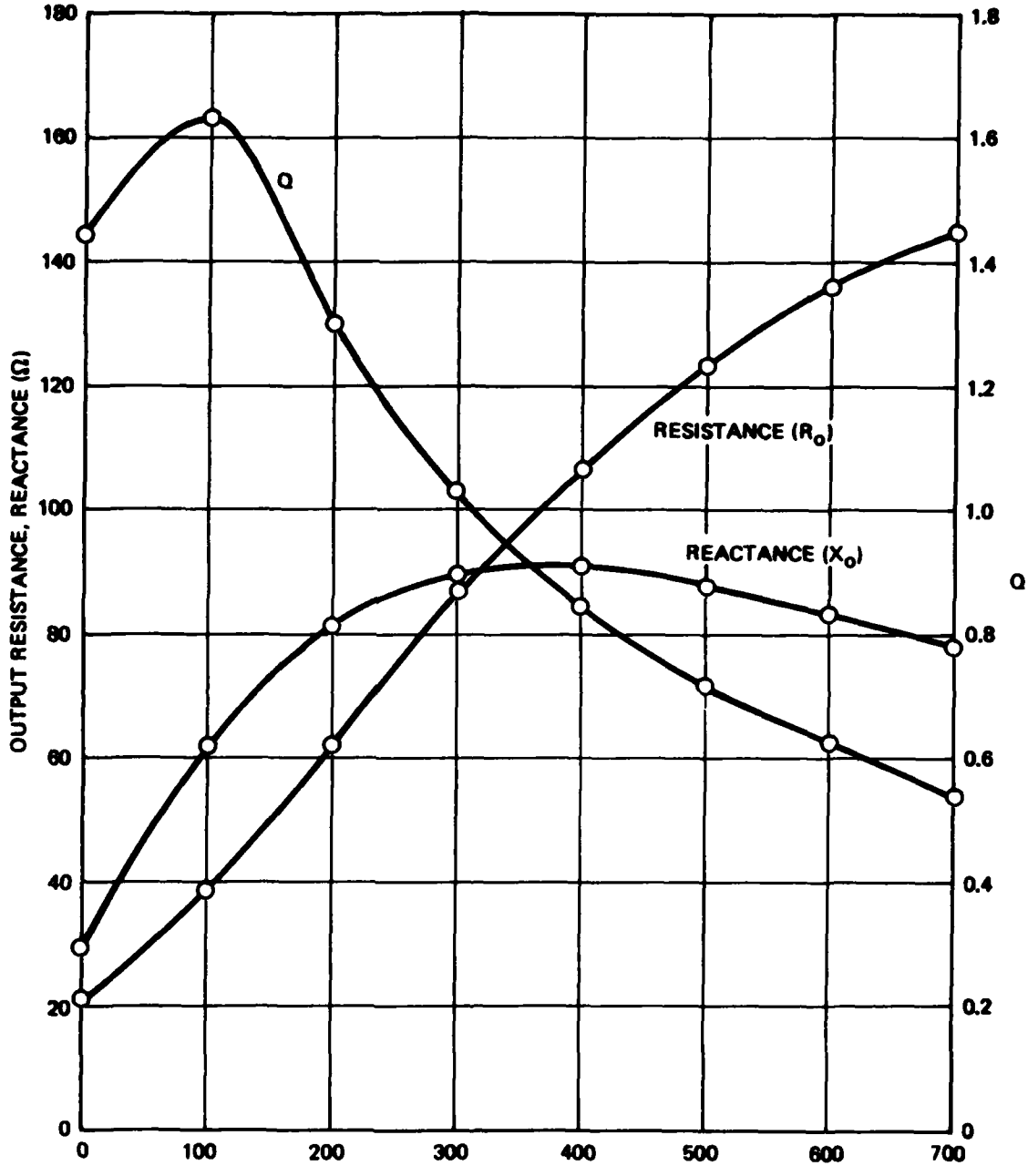


Figure (5.4). Output Resistance, Output Reactance, and Inductor Q for OAT 2T2L12W3 Device.

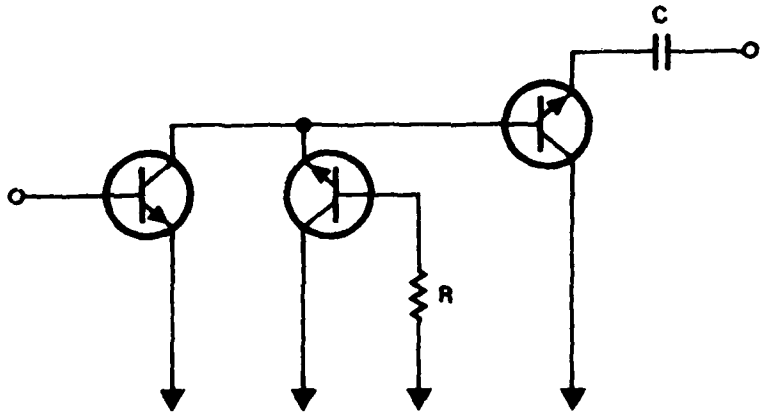


Figure (5.5). Signal Path for One Gain Stage.

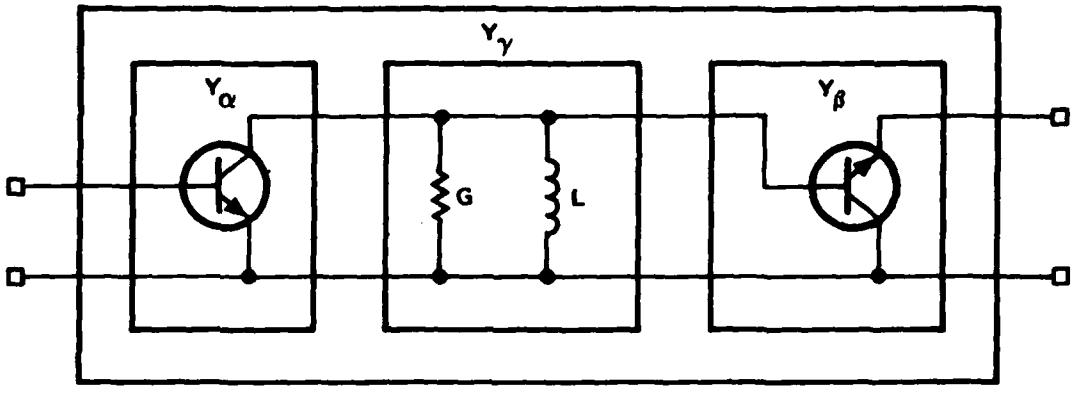


Figure (5.6). Two-Port Representation of Gain Path.

$$y_{11c} = y_{11\alpha} - \frac{y_{12\alpha}y_{21\alpha}}{y_{22\alpha} + y_{11\beta} + G + jB} \tag{5-13}$$

$$y_{22c} = y_{22\beta} - \frac{y_{12\beta}y_{21\beta}}{y_{22\alpha} + y_{11\beta} + G + jB} \tag{5-14}$$

$$y_{21c} = \frac{-y_{21\alpha}y_{21\beta}}{y_{22\alpha} + y_{11\beta} + G + jB} \tag{5-15}$$

$$y_{12c} = \frac{-y_{12\alpha}y_{12\beta}}{y_{22\alpha} + y_{11\beta} + G + jB} . \tag{5-16}$$

The power gain for the composite two port is given by

$$G_p = \frac{|y_{21c}|^2 \mathrm{Re}(Y_L)}{|Y_L + y_{22c}|^2 \mathrm{Re}\left(y_{11c} - \frac{y_{12c}y_{21c}}{y_{22c} + Y_L}\right)} \tag{5-17}$$

where

$$Y_L = \frac{1}{R_{IN} + j\left(X_{IN} - \frac{1}{\omega c}\right)} \tag{5-18}$$

is the admittance of the load network which consists of a coupling capacitor and the input to the next amplifier stage. In (5-18), $(R_{IN} + jX_{IN})$ is the input impedance of the driven stage. The power gain can be optimized by maximizing $|y_{21c}|^2$ followed by proper selection of coupling capacitance. However, this approach does not yield G_{MAX}, the maximum available gain, since the load network topology is not capable of conjugately matching the driver stage to the driven stage.

Table (5.1) is a list of y-parameters for both a common-emitter (Y_α) and common collector (Y_β) transistor at 1.6 GHz. These parameters are obtained from SPICE-2 simulations for which the transistor model of figure (5.7) is used. Using values from Table (5.1) in (5-15), one obtains

$$|y_{21c}|^2 = \frac{7.363 \times 10^{-7}}{D} \tag{5-19}$$

where

$$D = (1.179 \times 10^{-2} + G)^2 + (9.277 \times 10^{-3} + B)^2. \tag{5-20}$$

The maximum of $|y_{21c}|^2$ occurs at the minimum of the function D. Table (5.2) shows the dependence of D on the external base resistance of ICC transistor. This table is constructed from figure (5.4) and in particular,

$$G = \frac{1}{R_0(1 + Q^2)} \tag{5-21}$$

and

$$B = GQ. \tag{5-22}$$

These equations convert a series R-L impedance into a parallel G-L conductance at a single frequency. The table indicates that $|y_{21c}|^2$ is a maximum with an external base resistance of 300Ω. Note that $|y_{21c}|^2$ varies by only 14% as R_B varies between 100 and 400 ohms. The reason for this relative insensitivity to base resistance is that $(1.179 \times 10^{-2} + G)^2$ decreases and $(9.277 \times 10^{-2} + B)^2$ increases with increasing R_B resulting in a nearly constant value of D. In other words, as R_B increases above 150Ω, the resulting excess of inductance is compensated by the decrease in inductor conductivity. With $R_B \approx 150\Omega$, the inductance cancels the parallel parasitic capacitance.

TABLE (5.1)

Y-PARAMETERS FOR COMMON EMITTER AND

COMMON COLLECTOR CONFIGURATIONS AT 1.6 GHz

COMMON EMITTER

y_{11} = .01002 + j.005615

y_{12} = -.0004608 - j.001667

y_{21} = .003118 - j.02946

y_{22} = .001979 + j.003601

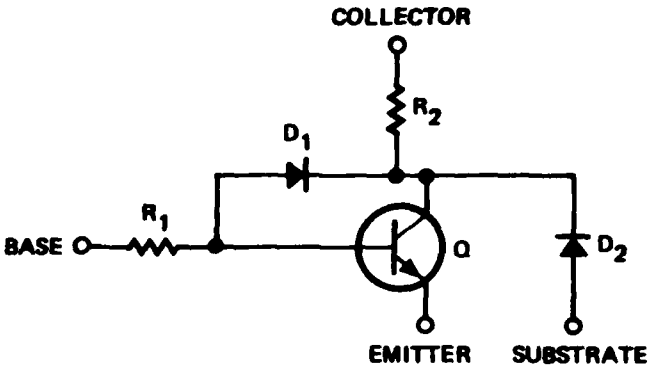
COMMON COLLECTOR

y_{11} = .009811 + j.005676

y_{12} = -.009455 - j.004072

y_{21} = -.01528 + j.02462

y_{22} = .01656 - j.02393



MODEL PARAMETERS

R_1 = 16Ω

R_2 = 34Ω

DIODE D_1:

CJO = .38 pf

PB = .7

M = .33

DIODE D_2:

CJO = .4 pf

PB = .7

M = .5

TRANSISTOR 1:

CJE = .16 pf

CJC = .039 pf

RB = 80Ω

RC = 60Ω

RE = 1Ω

TF = 24 ps

DELAY = 25 ps

BF = 60

IK = 12 mA

VA = 15V

IS = 2.0×10^{-16}A

Figure (5.7). SPICE-2 Macromodel for the 2T2L12W3 Transistor.

TABLE (5.2)

DEPENDENCE OF D ON EXTERNAL BASE RESISTANCE

R_B	G ($x10^3$)	-B ($x10^3$)	D ($x10^4$)
100	7.246	11.81	3.688
150	6.329	9.524	3.284
200	5.988	7.813	3.182
250	5.714	6.579	3.137
300	5.618	5.814	3.150
350	5.525	5.155	3.168
400	5.464	4.608	3.195

Using 300Ω as the ICC external resistor, y-parameters at 1.6 GHz for one gain stage become

$$\left.\begin{aligned} y_{11c} &= 1.270 \times 10^{-2} + j4.559 \times 10^{-3} \\ y_{22c} &= 5.134 \times 10^{-3} - j1.168 \times 10^{-2} \\ y_{21c} &= -4.342 \times 10^{-2} - j2.094 \times 10^{-2} \\ y_{12c} &= -7.451 \times 10^{-5} - j9.971 \times 10^{-4} \end{aligned}\right\} . \qquad (5\text{-}23)$$

The interstage network can be approximated by the circuit shown in figure (5.8). The voltage source, V_o, is the open circuit output voltage of the driver stage. It is assumed that the output impedance of the driving stage is approximately $1/y_{22c}$ and the input impedance of the driven stage is roughly $1/y_{11c}$. These approximations result in less than 10% error. The power delivered to the driven stage is

$$P_L = \frac{R_i V_o^2}{2[(R_o + R_i)^2 + (X_o + X_i - \frac{1}{\omega C})^2]} \qquad (5\text{-}24)$$

where

$$\left.\begin{aligned} R_o &= \mathrm{Re}(1/y_{22c}) = 31.54\Omega \\ X_o &= \mathrm{Im}(1/y_{22c}) = 71.75\Omega \\ R_i &= \mathrm{Re}(1/y_{11c}) = 69.75\Omega \\ X_i &= \mathrm{Im}(1/y_{11c}) = -25.03\Omega \end{aligned}\right\} . \qquad (5\text{-}25)$$

The maximum of P_L in (5-24) occurs when

$$C = \frac{1}{\omega(X_i + X_o)} . \qquad (5\text{-}26)$$

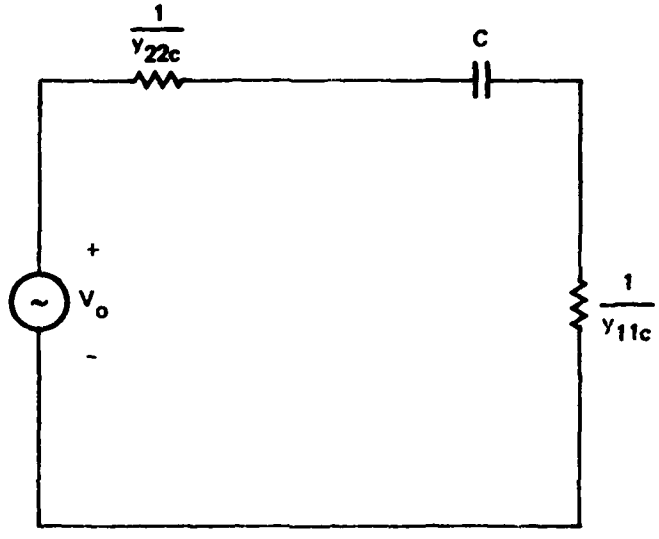


Figure (5.8). Interstage Network for RF Amplifier.

Using (5-25) and $\omega = (2\pi)(1.6 \times 10^9)$ in (5-26), the coupling capacitance becomes

$$C = 2.129 \text{ pf.} \tag{5-27}$$

Substituting (5-27) and (5-23) into (5-17) and (5-18), the power gain per stage becomes

$$G = 8.056 \text{ dB.} \tag{5-28}$$

5.1.3 Amplifier Design

The basic gain stage can be configured as the differential amplifier shown in figure (5.9). The complete amplifier consists of three cascaded differential stages with the output coupling capacitors omitted to conserve area. These capacitors are absorbed into the load circuit. The amplifier y-parameters, determined with SPICE-2, are used to determine the maximum available transducer gain given by

$$G_{MAX} = \frac{|y_{21}|^2}{2\text{Re}(y_{11})\text{Re}(y_{22}) - \text{Re}(y_{12}y_{21}) + \{[2\text{Re}(y_{11})\text{Re}(y_{22}) - \text{Re}(y_{12}y_{21})]^2 - |y_{12}y_{21}|^2\}^{\frac{1}{2}}} \tag{5-29}$$

Figure (5.10) is a plot of G_{MAX} as a function of frequency. Maximum gain is 32.2 dB and occurs at 1.2 GHz. The 3-dB bandwidth is 550 MHz.

To increase bandwidth and to desensitize the gain, a 50Ω resistor was inserted in series with each ICC transistor. This resistance is selected because it is the smallest resistor that can be easily integrated. The effect of this resistor is to increase the conductance of the ICC at the expense of enlarged reactive mismatch. The coupling

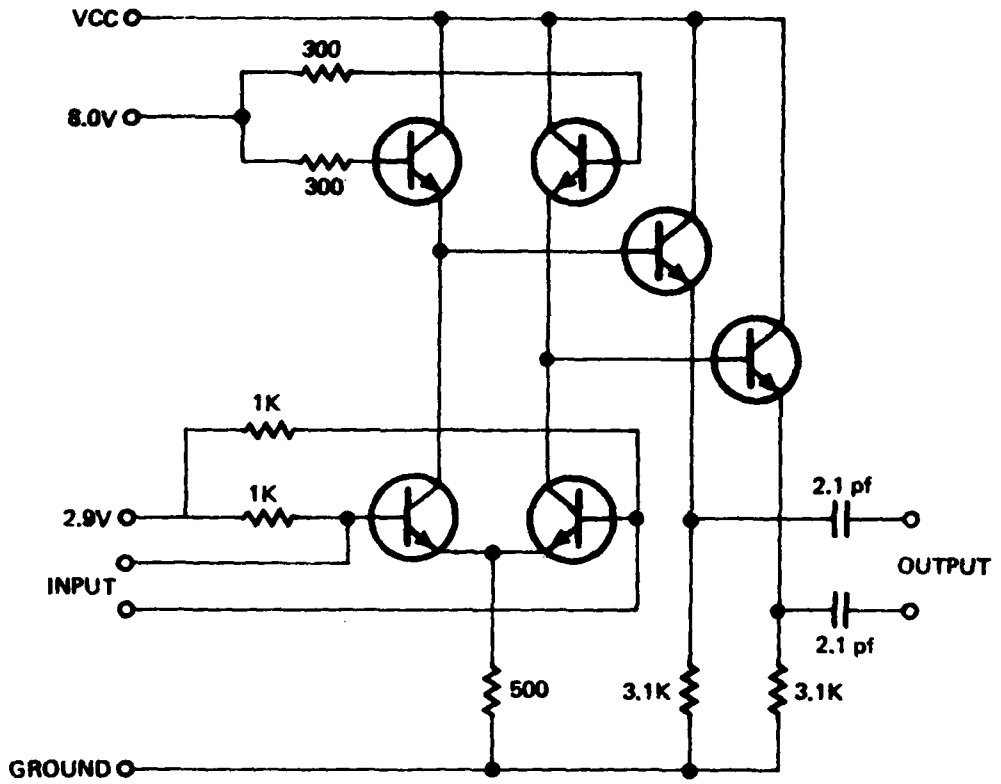


Figure (5.9). Differential Realization of Single Stage Amplifier.

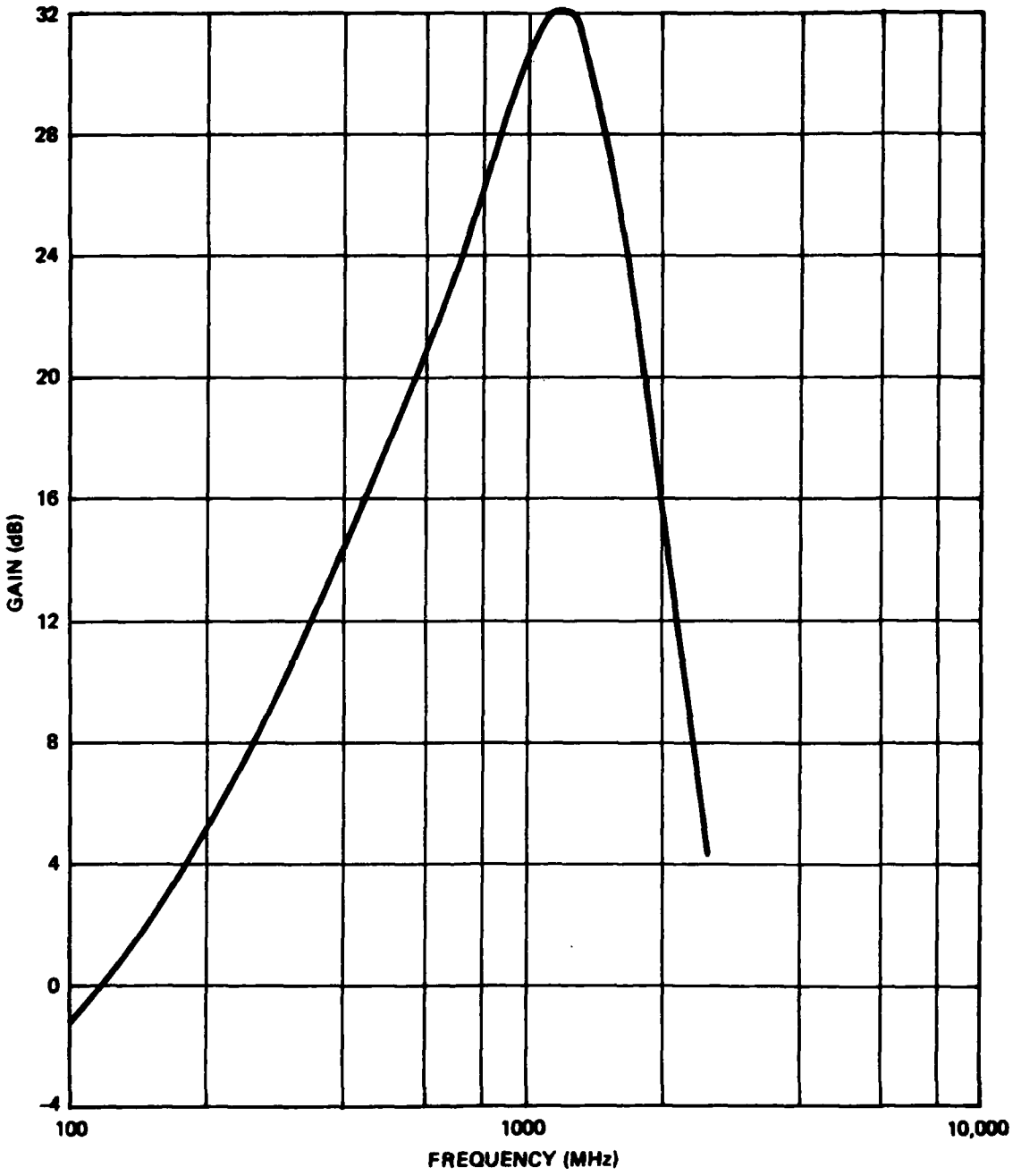


Figure (5.10). Simulated Frequency Response of G_{MAX}.

capacitors are reduced to 1.5 pf to conserve area. The ICC base resistor is adjusted for maximum gain after the changes described above are implemented. The frequency response of the final amplifier design is displayed in figure (5.11). Maximum gain is 29.6 dB and the resultant bandwidth is 800 MHz.

Table (5.3) shows the Linvill stability factor, C, input/output impedance, and input/output VSWR as a function of frequency. This table is constructed from the following set of equations:

$$C = \frac{|y_{12}y_{21}|}{2Re(y_{11})Re(y_{22}) - Re(y_{12}y_{21})}, \tag{5-30}$$

$$Z_{IN} = \left(y_{11} - \frac{y_{12}y_{21}}{y_{22} + Y_L}\right)^{-1}, \tag{5-31}$$

$$Z_{OUT} = \left(y_{22} - \frac{y_{12}y_{21}}{y_{11} + Y_S}\right)^{-1}, \tag{5-32}$$

and

$$VSWR_{IN,OUT} = \frac{1 + |\rho_{IN,OUT}|}{1 - |\rho_{IN,OUT}|}, \tag{5-33}$$

where

$$\rho_{IN,OUT} = \frac{Z_{IN,OUT} - 100}{Z_{IN,OUT} + 100}. \tag{5-34}$$

The characteristic impedance in the reflection coefficient equation is 100Ω because the amplifier is differential. Y_S and Y_L were set to .02℧ in (5-31) and (5-32) during the determination of Z_{IN}

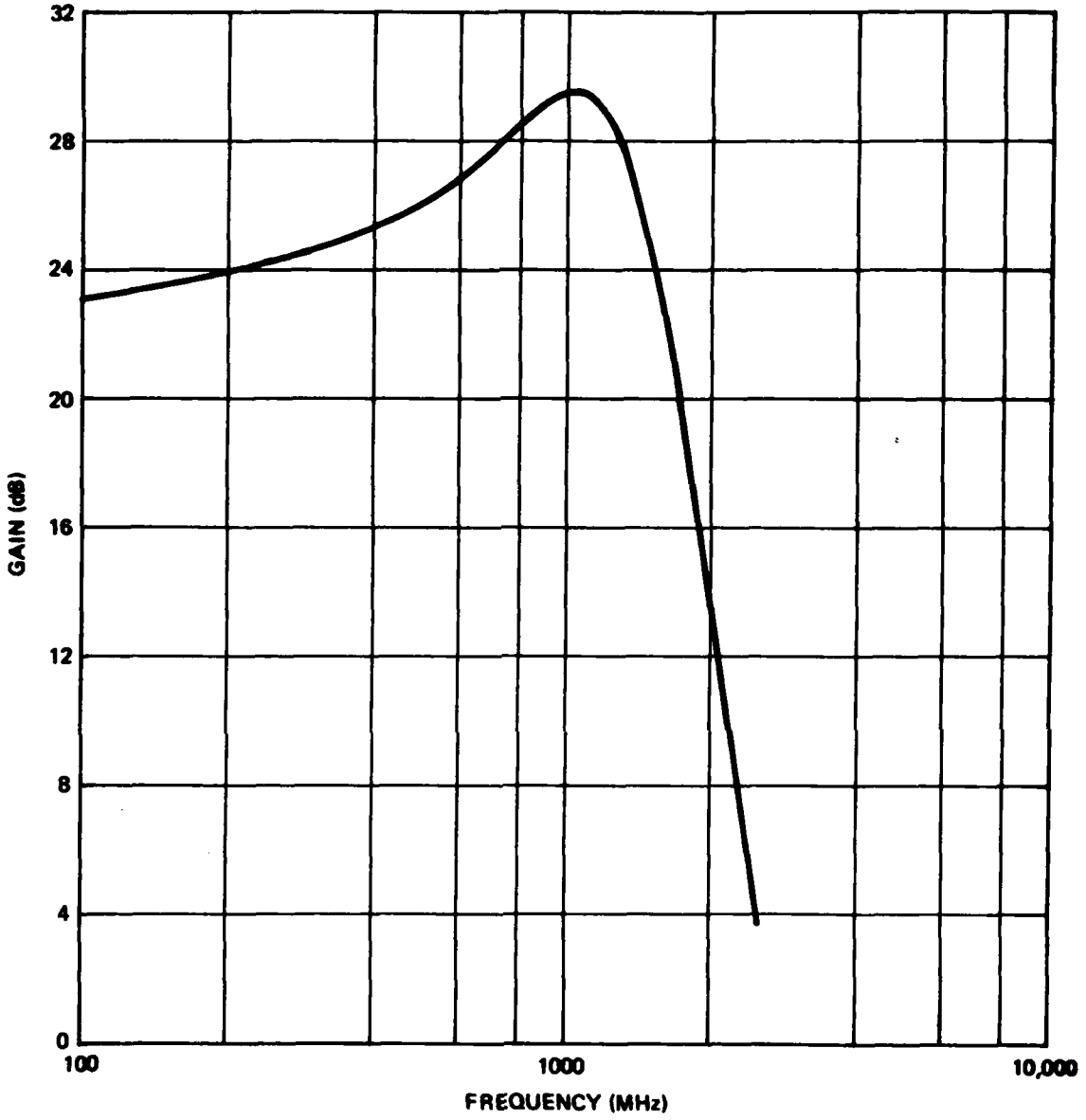


Figure (5.11). Final Response Achieved Subsequent to Circuit Changes Dictated by Fabrication Constraints.

TABLE (5.3)

AMPLIFIER PERFORMANCE PARAMETERS

FREQ (MHz)	C	$Z_{IN}(\Omega)$	Z_{OUT}	$VSWR_{IN}$	$VSWR_{OUT}$
100	7.40×10^{-11}	513 - j453	36.7 + j12.3	9.21	2.73
200	5.19×10^{-9}	253 - j342	36.3 + j12.3	7.42	2.80
300	6.57×10^{-8}	170 - j248	35.7 + j18.8	5.72	2.91
400	4.41×10^{-7}	139 - j189	35.0 + j25.8	4.45	3.07
500	2.14×10^{-6}	122 - j148	34.3 + j33.3	3.56	3.27
600	8.14×10^{-6}	114 - j119	33.8 + j41.4	2.91	3.51
700	2.84×10^{-5}	109 - j96.4	33.8 + j50.2	2.45	3.78
800	8.40×10^{-5}	107 - j78.1	34.3 + j59.7	2.10	4.06
900	2.19×10^{-4}	107 - j62.2	35.6 + j69.8	1.82	4.31
1000	4.97×10^{-4}	107 - j48.9	38.5 + j80.7	1.61	4.44
1100	9.67×10^{-4}	110 - j36.7	42.9 + j91.3	1.43	4.48
1200	1.56×10^{-3}	114 - j26.9	48.9 + j101	1.33	4.40
1300	2.23×10^{-3}	120 - j19.1	56.2 + j110	1.29	4.24
1400	2.70×10^{-3}	126 - j14.9	64.2 + j117	1.30	4.07
1500	2.95×10^{-3}	131 - j11.8	71.4 + j122	1.33	3.94
1600	3.01×10^{-3}	135 - j9.61	78.9 + j127	1.37	3.84
1700	2.92×10^{-3}	139 - j9.36	84.8 + j131	1.40	3.79
1800	2.76×10^{-3}	142 - j7.82	91.5 + j135	1.43	3.74
1900	2.56×10^{-3}	144 - j7.43	96.5 + j139	1.45	3.73
2000	2.35×10^{-3}	146 - j7.68	103 + j143	1.47	3.71

and Z_{OUT} in Table (5.3). The amplifier is unconditionally stable since the C factor is less than one. Actually, C is not calculated for frequencies below 100 MHz. However, $|y_{12}| < 10^{-14}$ for frequencies below 100 MHz which should render a stable amplifier.

5.2 IF Amplifier

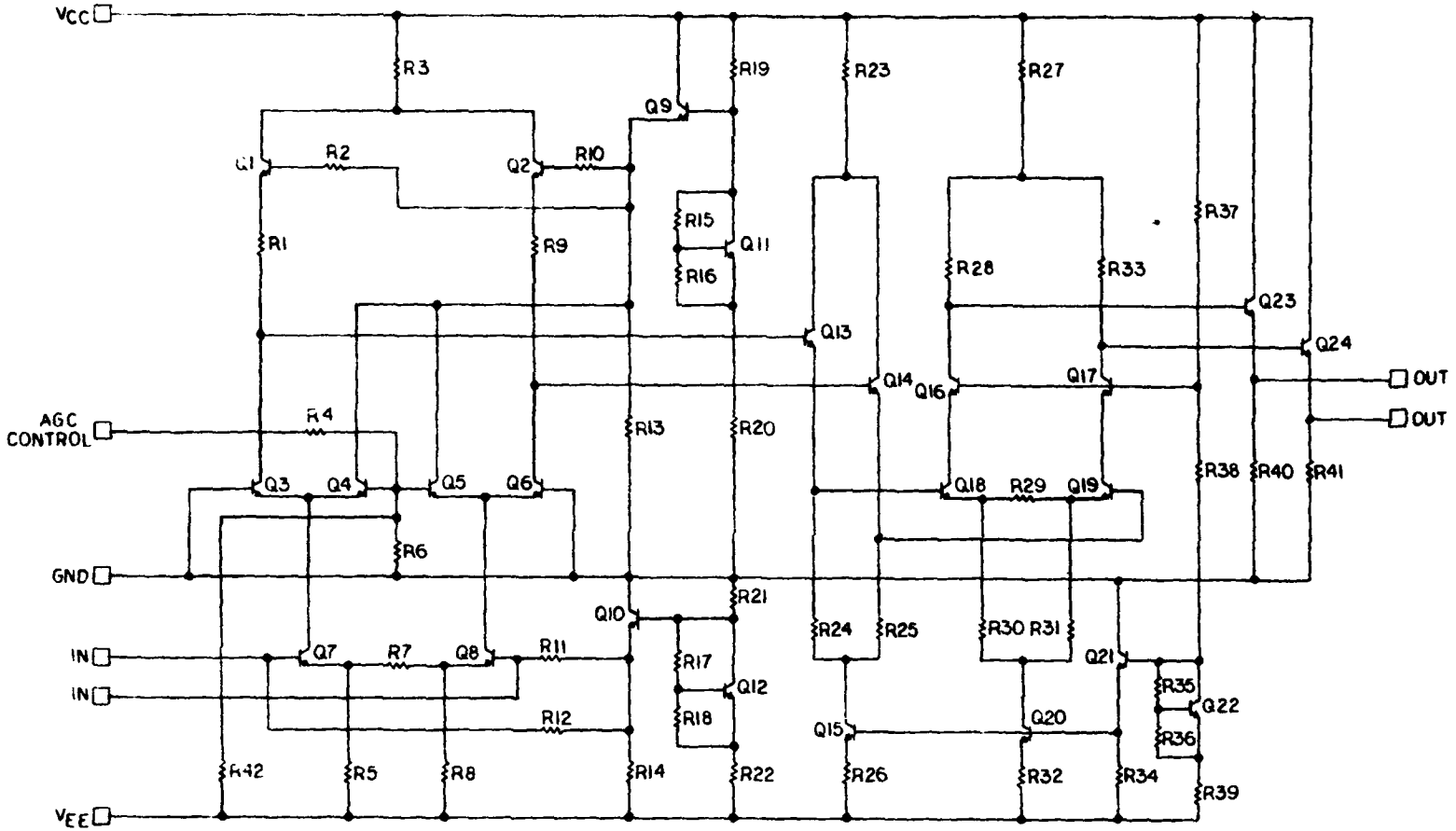
The schematic diagram of the IF amplifier is shown in figure (5.12). The circuit consists of two cascaded differential pairs operating in a cascode configuration (Q_3 - Q_6 - Q_7 - Q_8; Q_{16} - Q_{19}). The first gain stage is shunt-peaked by means of the output inductance of Q_1 and Q_2. Emitter followers Q_{13}, Q_{14}, Q_{23}, Q_{24} buffer each gain stage. Transistors Q_{23} and Q_{24} are biased to deliver -10 dBm into a 50Ω load. Automatic gain control of the amplifier is accomplished by varying the bias of Q_4 and Q_5. Gain is decreased by increasing the bias current of these transistors via an increase in AGC control voltage. Transistors Q_9 - Q_{12}, Q_{15}, Q_{20} - Q_{22} provide temperature-compensated biasing.

5.2.1 Frequency Response

The voltage gain as a function of frequency was simulated on SPICE-2 for the case of capacitively coupled 50 ohm load resistors. Figure (5.13) shows the computer results. The voltage gain is 30 dB and the 3-dB bandwidth is 370 MHz.

The differential impedance of the input and output ports was simulated. A differential current source was applied to the port under test while the other port was determined with a 100Ω resistor. The results are offered as Table (5.4).

The common mode gain of the amplifier was also simulated. The common mode rejection ratio (CMRR) is plotted in figure (5.14) as a function of frequency.



RESISTOR VALUES ARE IN OHMS AT 200 OPS.

R1,9,28,33 = 400
R2,10,11,12 = 2K
R3,26,32 = 1.6K
R4 = 200
R5,8 = 1.0K
R7,29 = 50
R13 = 4.5K
R14 = 1.8K
R15 = 2.11K
R16,18,36 = 750
R17 = 1.06K
R19 = 3.22K
R20 = 1.19K
R21 = 1.7K
R22 = 356
R23 = 2.2K
R24,25 = 1.3K
R27 = 800
R30,31 = 500
R34 = 3.9K
R35 = 1.1K
R37 = 2.56K
R38 = 3.88K
R39 = 1.4K
R40,41 = 2.3K
R6 = 3.5K
R42 = 2.5K

RFCS-1
IF AMPLIFIER
(9)

NOTES:
1. V_{CC} +12.0VDC
2. V_{EE} -6.0 VDC
3. INPUT AND OUTPUT PADS ARE 4 MILS IN DIAMETER
4. P_D = 308 mw

DEVICE TYPES
Q15, 20 = 2T2LI2W3
Q23, 24 = 2T4LI2W3
ALL OTHERS = 2TILI2W3

APPROVED
Dennis Lewis 5-22-79
Div Engrs 22 MAY 79

Figure (5.12). Schematic Diagram of IF Amplifier.

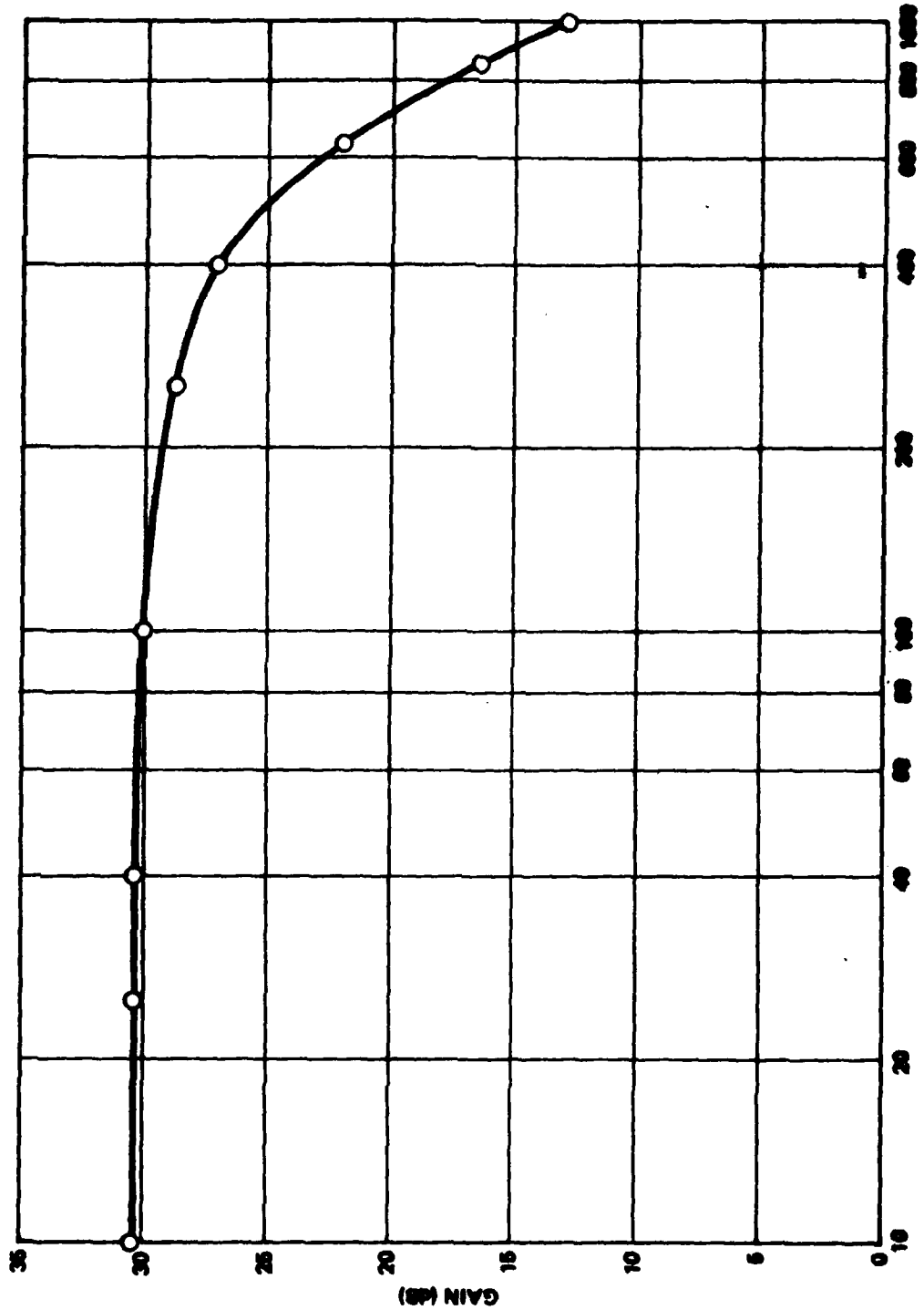


Figure (5.13). Simulated Frequency Response of IF Amplifier.

TABLE (5.4)

INPUT AND OUTPUT IMPEDANCES

FOR IF AMPLIFIER

INPUT PORT

Freq (MHz)	$Z_{IN}(\Omega)$
10	2550 - j1780
100	1710 - j1140
250	708 - j973
400	429 - j698
630	300 - j455

OUTPUT PORT

Freq (MHz)	$Z_{OUT}(\Omega)$
10	44.5 + j2.44
100	49.1 + j23.7
250	67.9 + j51.3
400	91.3 + j64.9
630	122 + j67.5

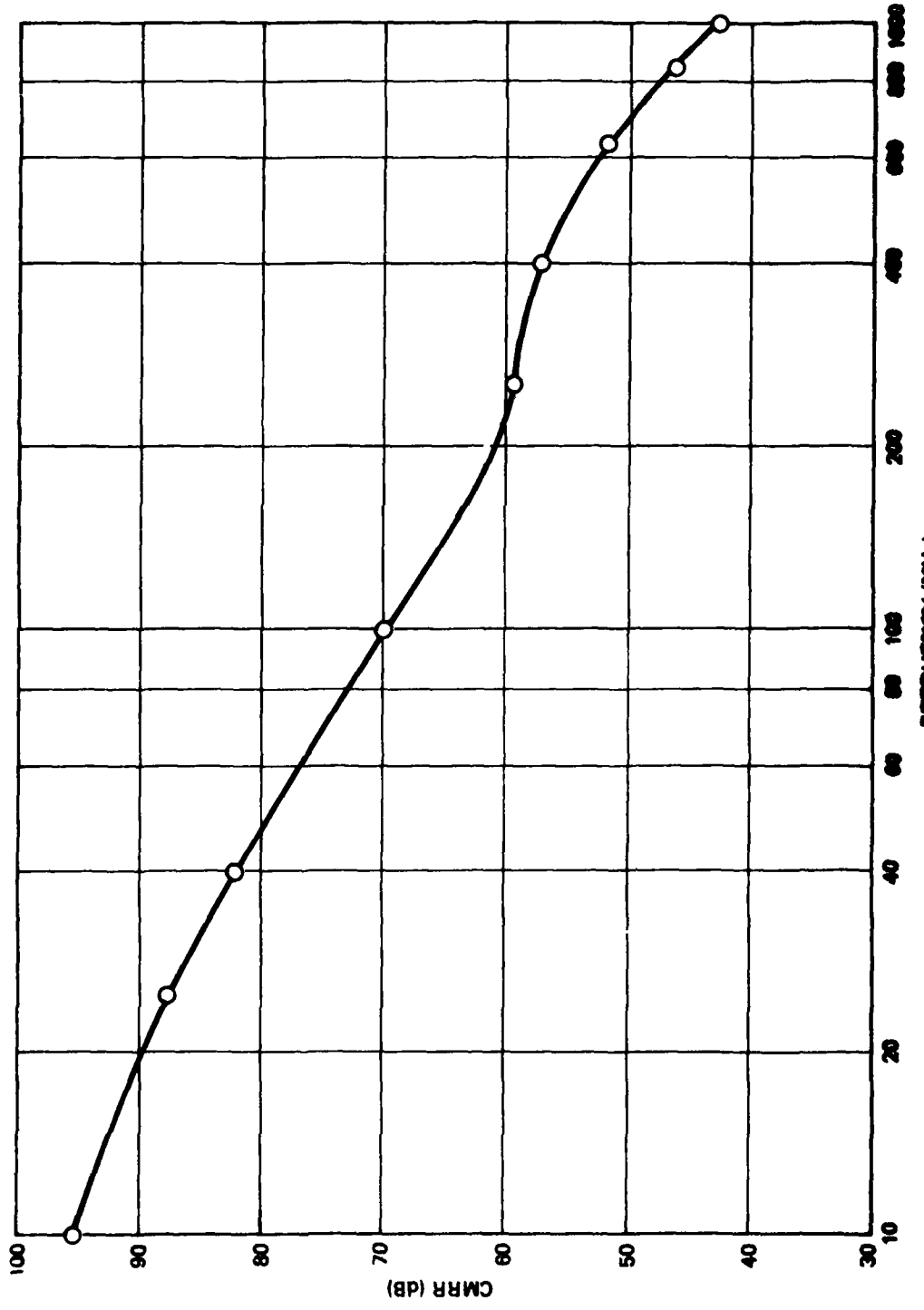


Figure (5.14). CMRR Response of IF Amplifier.

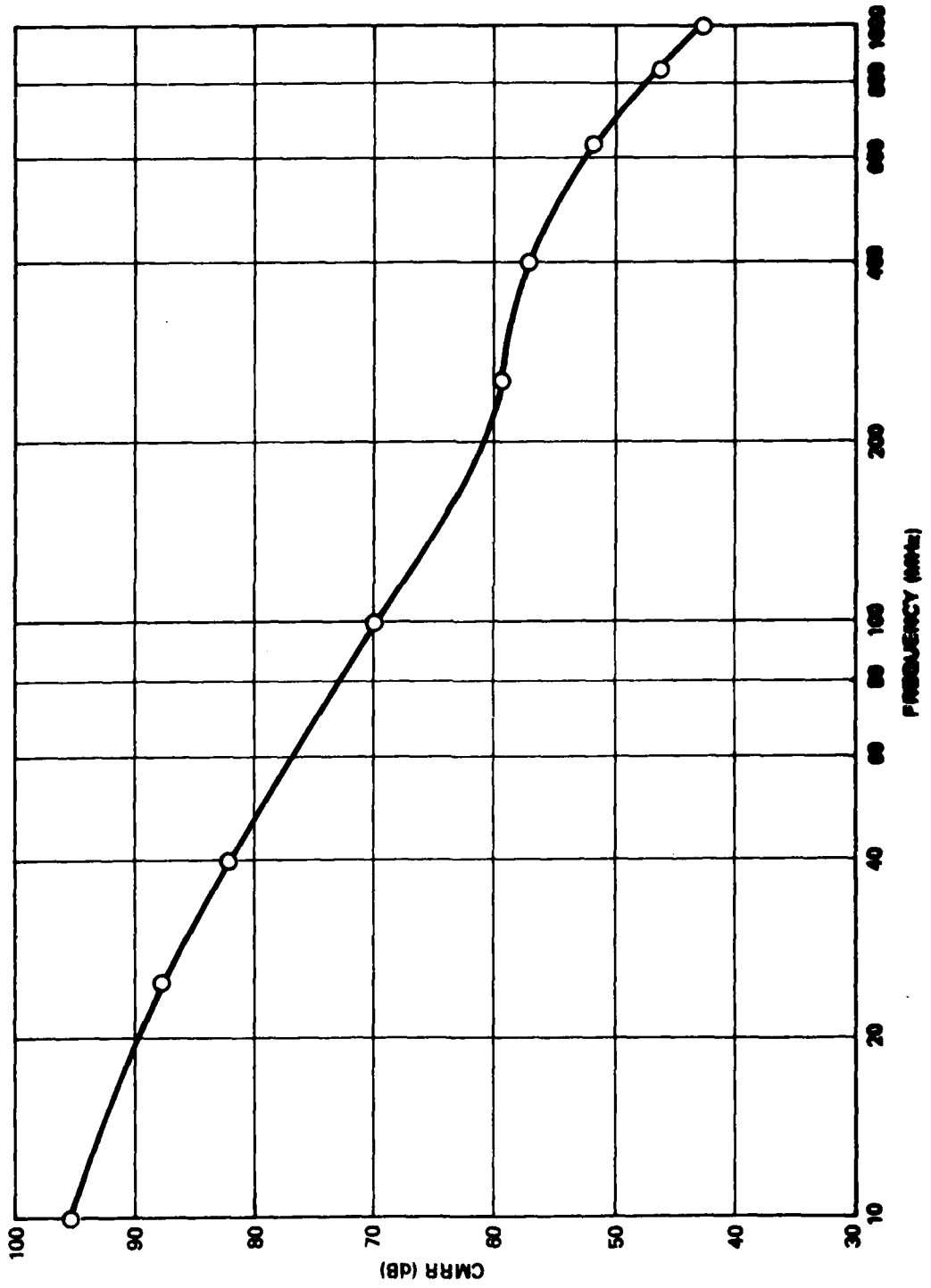


Figure (5.14). CMRR Response of IF Amplifier.

5.2.2 Automatic Gain Control

The AGC capability of the amplifier was investigated only for the case of very low frequencies at dc for simulation ease. As a result, the coupling capacitors are open circuits and since the 50Ω load resistors are capacitively coupled, the gain determined in this analysis is larger than the low frequency, loaded gain by a factor of

$$20 \log\left(\frac{R_o + 50}{50}\right) \approx 20 \log\left(\frac{20 + 50}{50}\right)$$

$$\approx 2.9 \text{ dB},$$

where R_o is the output resistance of Q_{23} and Q_{24}. Figure (5.15) shows a plot of gain versus AGC voltage. The AGC range is in excess of 40 dB.

SPICE-2 OAT macromodel parameters used in all computer analyses are given in Table (5.5). Figure (5.7) defines the macromodel topology.

5.3 Analog Multiplier

The analog multiplier shown in figure (5.16) is a standard transconductance multiplier cell (Q_y - Q_{11}) utilizing cascode transistors (Q_4, Q_5). Emitter followers (Q_{17}, Q_{18}) are provided to drive 50Ω loads. Resistors R_{15} - R_{18} are laser trimmable to null offsets. Transistors Q_{12} - Q_{16} and Q_{19} provide temperature-compensated biasing.

5.3.1 Circuit Design

The circuit is designed to have a conversion gain of at least 0 dB when the LO signal rests at its maximum amplitude. Since the multiplier output voltage is expressible as

$$V_O = KV_{LO}V_{SIGNAL}, \qquad (5\text{-}35)$$

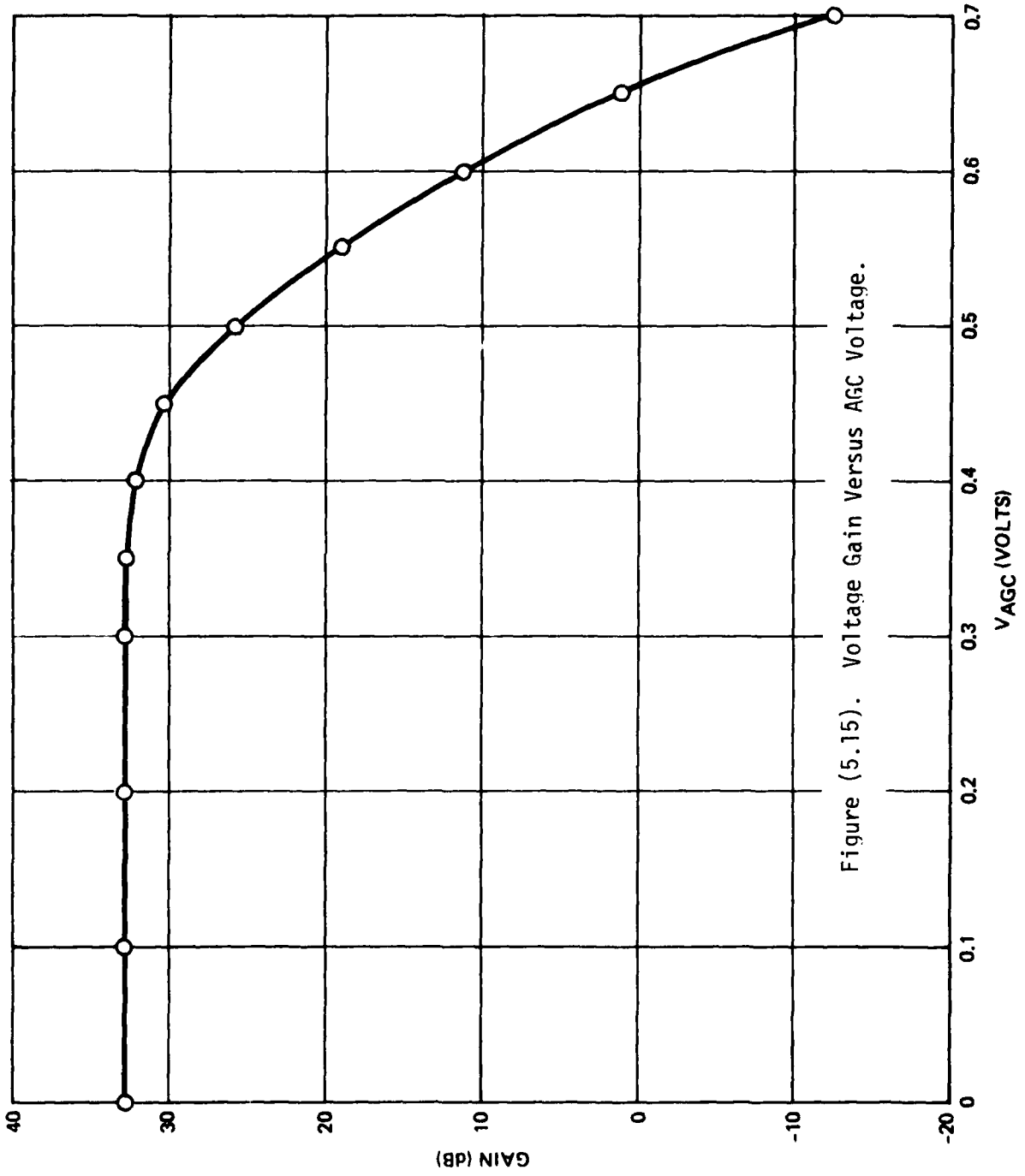


Figure (5.15). Voltage Gain Versus AGC Voltage.

TABLE (5.5)

SPICE-2 OAT MODEL PARAMETERS (IF)

TRANSISTOR 2T4L12W3

R1: 8Ω
R2: 17Ω

Diode DCB		Diode DCS	
CJO	= .6 pf	CFO	= .6 pf
PB	= .7 volts	PB	= .7 volts
M	= .33	M	= .5

Transistor Q_1

CJC	= .08 pf	BF	= 60
CJE	= .32 pf	DELAY	= 25 ps
RB	= 40Ω	TF	= 24 ps
RE	= 2Ω	IK	= 8 mA
RC	= 30Ω	IS	= 2×10^{-16} A
VA	= 15 volts		

TRANSISTOR 2T2L12W3

R1: 16
R2: 34

Diode DCB		Diode DCS	
CJO	= .38 pf	CJO	= .4 pf
PB	= .7 volts	PB	= .7 volts
M	= .33	M	= .5

TABLE (5.5) (CONT'D)

TRANSISTOR 2T2L12W3 (CONT'D)

Transistor Q_1

CJC	= .039 pf	BF	= 60
CJE	= .16 pf	DELAY	= 25 ps
RB	= 80Ω	TF	= 24 ps
RE	= 2Ω	IK	= 8 mA
RC	= 60Ω	IS	= 2×10^{-16} A
VA	= 15 volts		

TRANSISTOR 2T1L12W3

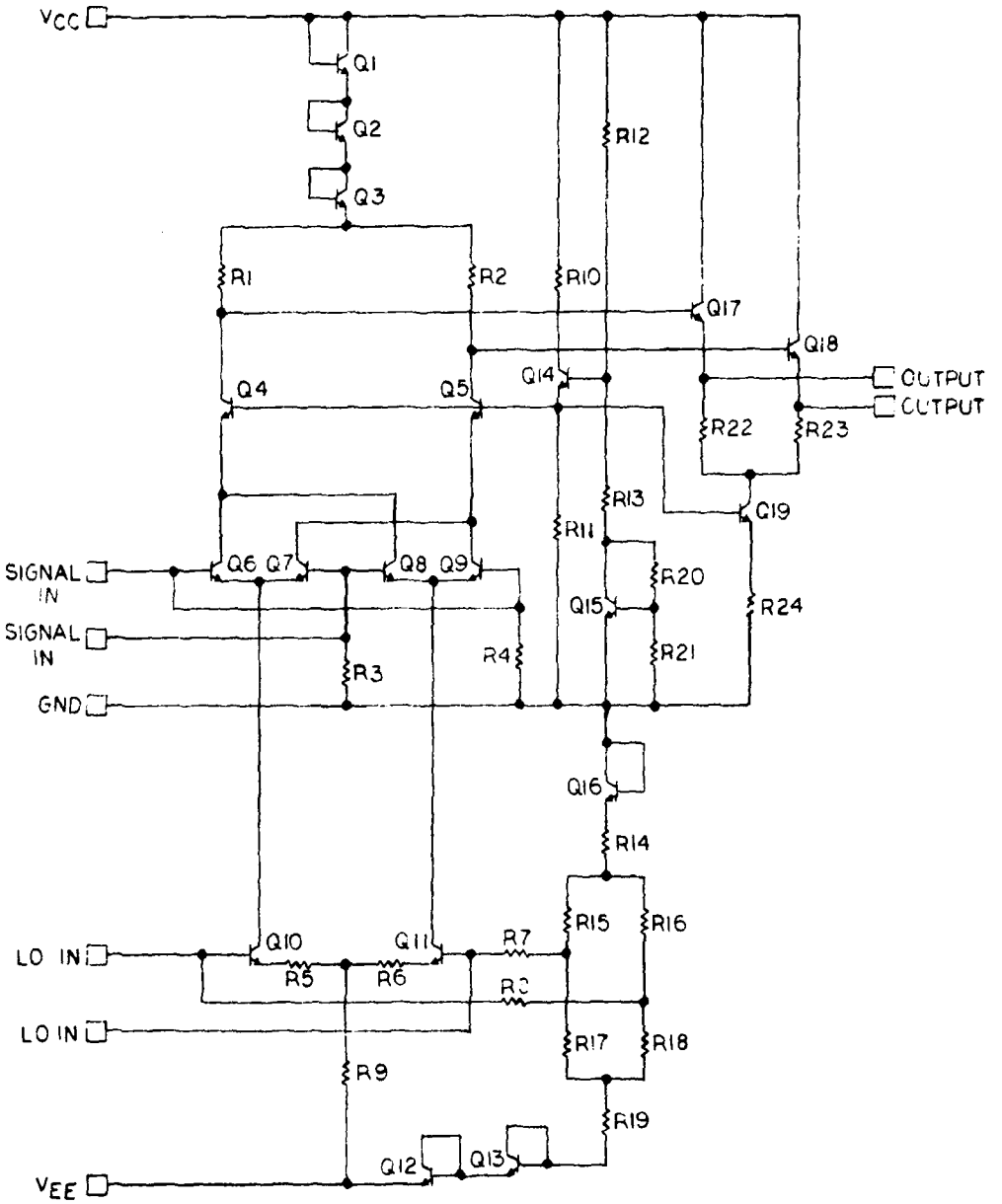
R1: 32

R2: 68

Diode DCB		Diode DCS	
CJO	= .25 pf	CJO	= .3 pf
PB	= .7 volts	PB	= .7 volts
M	= .33	M	= .5

Transistor Q_1

CJC	= .02 pf	BF	= 60
CJE	= .08 pf	DELAY	= 25 ps
RB	= 160Ω	TF	= 24 ps
RE	= 2Ω	IK	= 8 mA
RC	= 120Ω	IS	= 2×10^{-16} A
VA	= 15 volts		



RESISTOR VALUES ARE IN OHMS AT 200 OPS

R1-6,15-18=100
R7,8 = 2K
R9=400
R10=3K
R11=5.2K
R 2=4K
R13=2.4K
R14=2.5K
R19=1.3K
R20=3.3K
R21=1.5K
R22,23=1K
R24=1.1K

DEVICE TYPES

Q1,2,3,19 = 2T2L17W3
Q6-Q9,Q12-Q16=2TIL12W3
Q4,5,10,11,17,18=2T2L12W3

RFCS-1
ANALOG MULTIPLIER

APPROVED

Dennis Cocco 17 May 79

DRAWN-16 MAY 79

NOTES:

1. V_{CC} = +12.0 VDC
2. V_{EE} = -6.0 VDC
3. R15-18 ARE LASER TRIMMABLE. (L = 3GRIDS + 3% COMP W=6 GRIDS)
4. INPUT & OUTPUT PADS ARE 4 MILS IN DIAMETER.
5. P_D = 158 mw

Figure (5.16). Schematic Diagram of Analog Multiplier.

with K representing a scale factor, a conversion gain of 0 dB is realized if

$$KV_{LO} = 1. \tag{5-36}$$

For minimum distortion, the differential LO signal voltage must satisfy

$$V_{LO} \leq .01(1 + .038R_E)^2. \tag{5-37}$$

This value is obtained by making the first order term in a power series expansion of collector current equal to ten times the value of the second order term.

For $R_E = 100$, (5-37) delivers

$$V_{LO} \leq .24\ V. \tag{5-38}$$

Therefore,

$$K \geq 4.2. \tag{5-39}$$

SPICE-2 predicts a K value of 6.2 at low frequencies, which implies sufficient margin.

5.3.2 Frequency Response

The simulated frequency response of both the LO port and signal port derives under the condition that a static voltage (1 millivolt) is applied to the signal port. Additionally, a 1 volt AC signal is connected to the LO port to determine the voltage gain versus frequency of the LO port. The signal sources are transposed to analyze the signal port response. Fifty ohm loads are present on both terminals in both simulations. Figures (5.17) and (5.18) show the computer results. The 3-dB K-factor bandwidths are 500 MHz and 600 MHz for signal port and LO port, respectively.

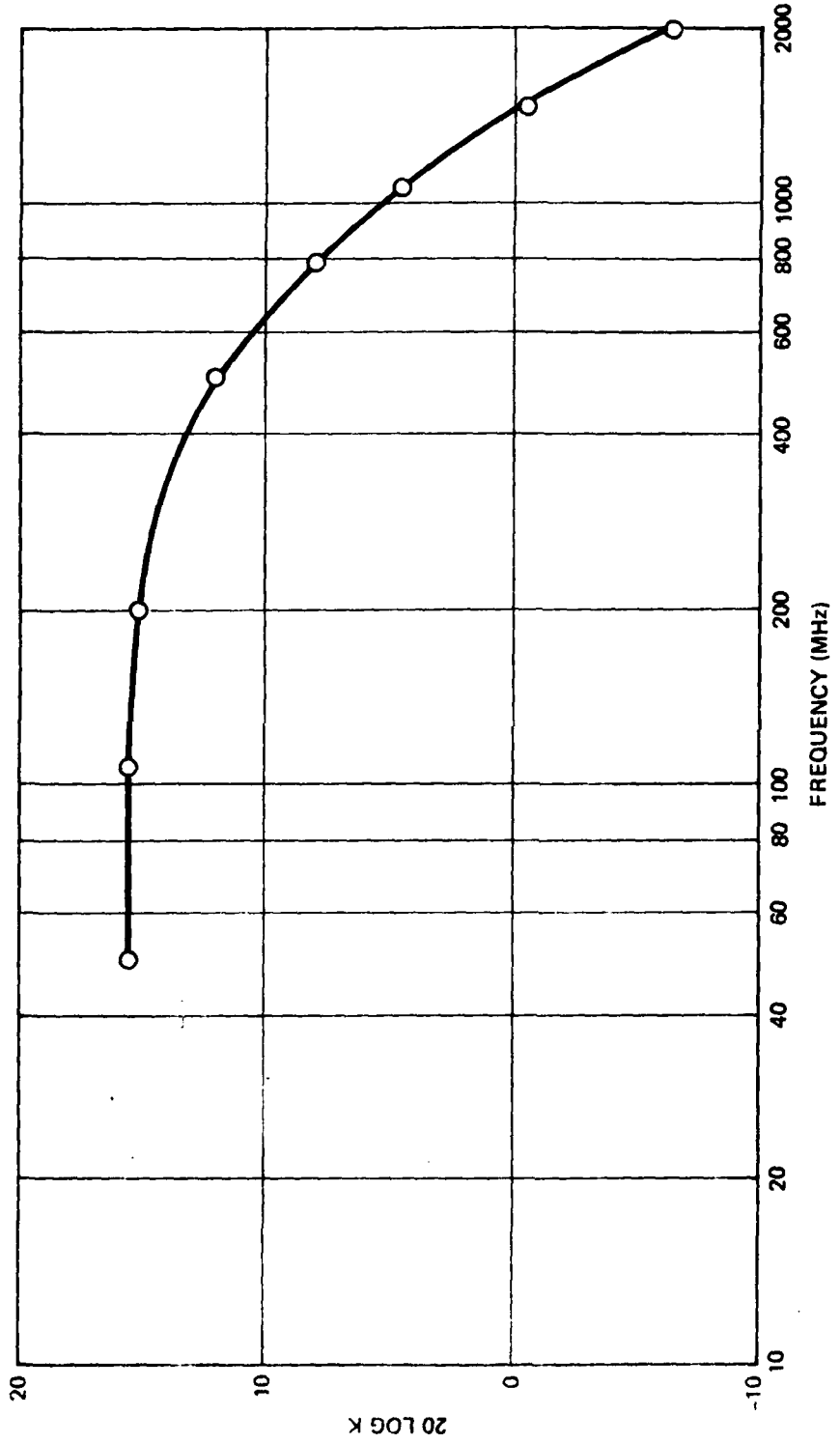


Figure (5.17). Signal Port Frequency Response.

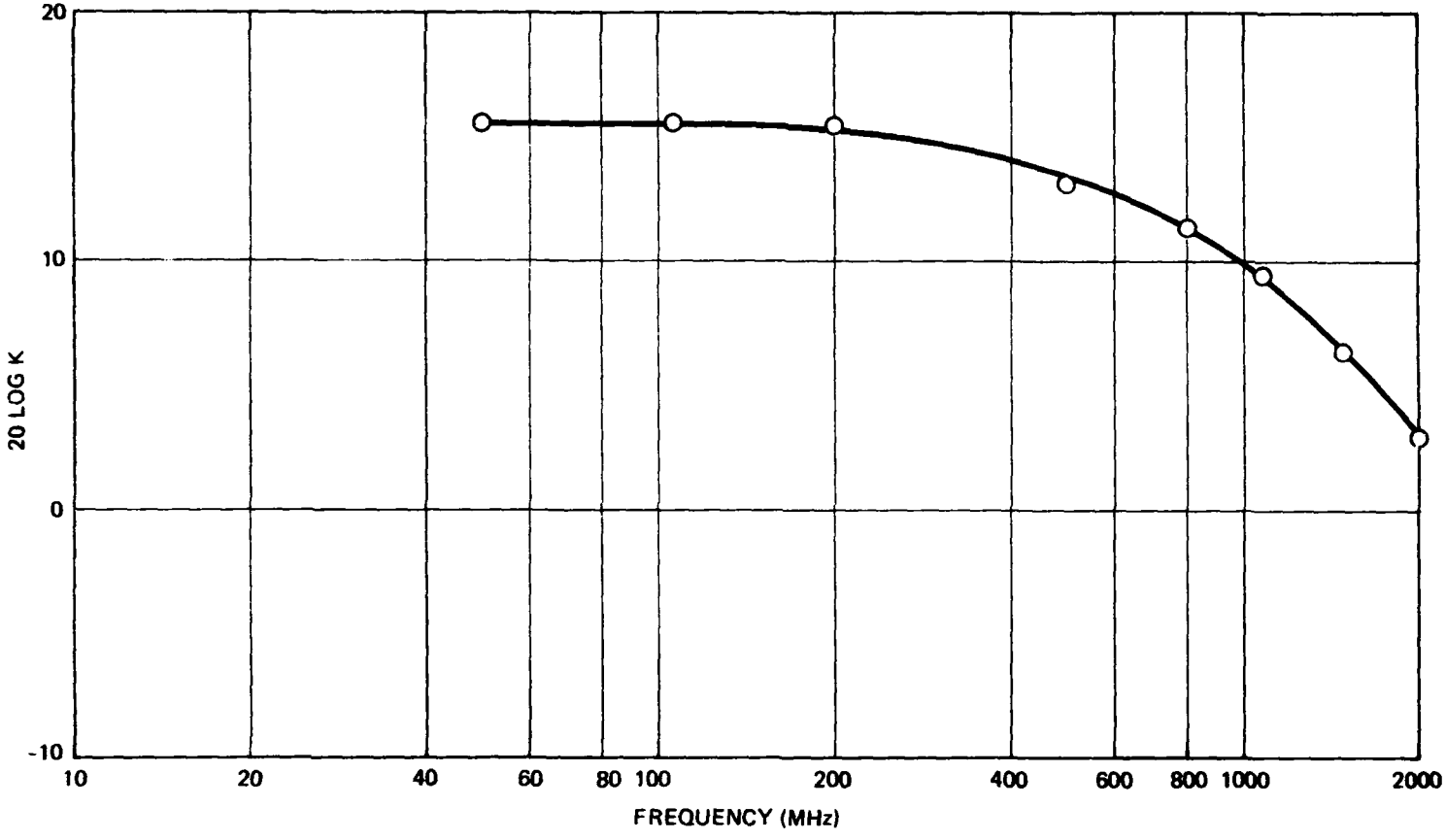


Figure (5.18). LO Port Frequency Response.

Table (5.6) lists the results of differential input impedance simulations at both the LO and signal port and the simulated differential output impedance. Table (5.7) defines the OAT bipolar model parameters pertinent to all simulations.

5.4 Operational Amplifier

The operational amplifier is depicted in figure (5.19). Transistors Q6 through Q21 comprise the basic gain cell, which appears in simplified format as figure (4.11). Transistors Q17, Q18, Q13, Q14, Q9 and Q10 correspond respectively to devices 3, 4, 5, 6, 9 and 10 in figure (4.11). Each of these six transistors is shunted by an identical transistor to equalize current distribution and hence to preclude excessive thermal gradients between the inner part of the cell and the outer cell component. The outer cell is composed of transistors Q20, Q21, Q6 and Q7, which correspond to devices 1, 2, 7 and 8, respectively in figure (4.11). Resistors R9 and R10 are load resistances for the cell whose function mirrors that of R_C in the basic configuration.

Transistor Q22 is the current sink for the inner portion of the gain cell, while Q3 through Q5 comprise a frequency compensated sink for the outer cell. Transistor Q22 conducts 1.66 mA, while Q5 conducts 570 μA under balanced condition. Since the ratio of these currents controls the negative resistance of the cell, and hence the gain and low frequency phase characteristics of the op-amp, external taps are provided at the emitters of Q4 and Q22 for fine adjustment of bias current ratio. The adjustment is effected through an appropriate resistor (>20 KΩ) connected from CUR. COMP. 1 and CUR. COMP. 2 to GND. These current sources, as well as the currents flowing through Q33 and Q34 are thermally compensated by the stabilized reference circuit comprised of Q1 and Q2.

Transistor pairs Q23-Q25 and Q24-Q26 are Darlington buffers driving the differential level shift circuit defined by Q27-Q29 and and Q28-Q30. The level shifter establishes a quiescent voltage at

TABLE (5.6)

SIMULATED CIRCUIT IMPEDANCES FOR MULTIPLIER

LO PORT

Freq (MHz)	$Z_{IN}(\Omega)$	VSWR (100Ω System)
100	2100 - j1400	30:1
500	370 - j830	23:1
1000	170 - j400	12:1
1500	140 - j290	8.0:1
2000	130 - j200	4.9:1

SIGNAL PORT

Freq (MHz)	$Z_{IN}(\Omega)$	VSWR (100Ω System)
100	180 - j24	1.8:1
500	120 - j48	1.6:1
1000	100 - j34	1.4:1
1500	90 - j28	1.4:1
2000	88 - j22	1.3:1

OUTPUT PORT

Freq (MHz)	$Z_{IN}(\Omega)$	VSWR (100Ω System)
100	42 + j9.6	2.4:1
500	50 + j43	2.5:1
1000	76 + j82	2.6:1
1500	96 + j100	2.7:1
2000	120 + j120	2.9:1

TABLE (5.7)

OAT TRANSISTOR MACROMODEL PARAMETERS (MULTIPLIER)

TRANSISTOR 2T2L17W3

R1: 8Ω
R2: 17Ω

Diode DCB

CJO = .6 pf
PB = .7 volts
M = .33

Diode DCS

CJO = .6 pf
PB = .7 volts
M = .5

Transistor Q_1

CJC = .08 pf
CJE = .32 pf
RB = 40Ω
RE = 2Ω
RC = 30Ω
VA = 15 volts

BF = 60
DELAY = 25 ps
TF = 24 ps
IK = 8 mA
IS = 2×10^{-16} A

TRANSISTOR 2T2L12W3

R1: 16
R2: 34

Diode DCB

CJO = .38 pf
PB = .7 volts
M = .33

Diode DCS

CJO = .4 pf
PB = .7 volts
M = .5

TABLE (5.7)

(CONTINUED)

TRANSISTOR 2T2L12W3 (CONT'D)

Transistor Q_1

CJC	= .039 pf	BF	= 60
CJE	= .16 pf	DELAY	= 25 ps
RB	= 80Ω	TF	= 24 ps
RE	= 2Ω	IK	= 8 mA
RC	= 60Ω	IS	= 2×10^{-16} A
VA	= 15 volts		

TRANSISTOR 2T1L12W3

R1: 32

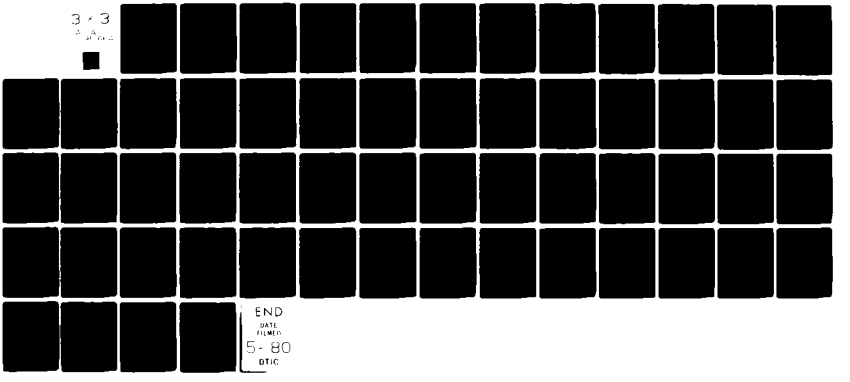
R2: 68

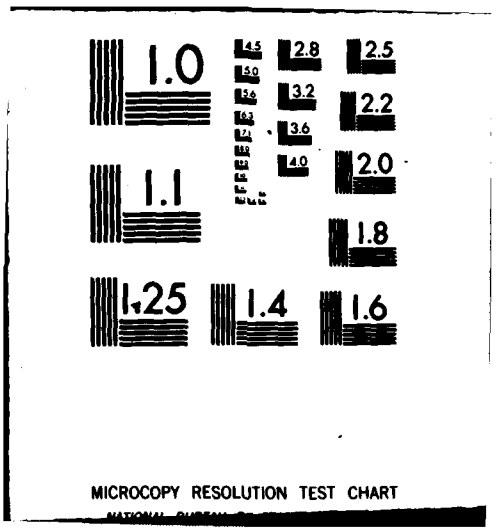
Diode DCB		Diode DCS	
CJO	= .25 pf	CJO	= .3 pf
PB	= .7 volts	PB	= .7 volts
M	= .33	M	= .5

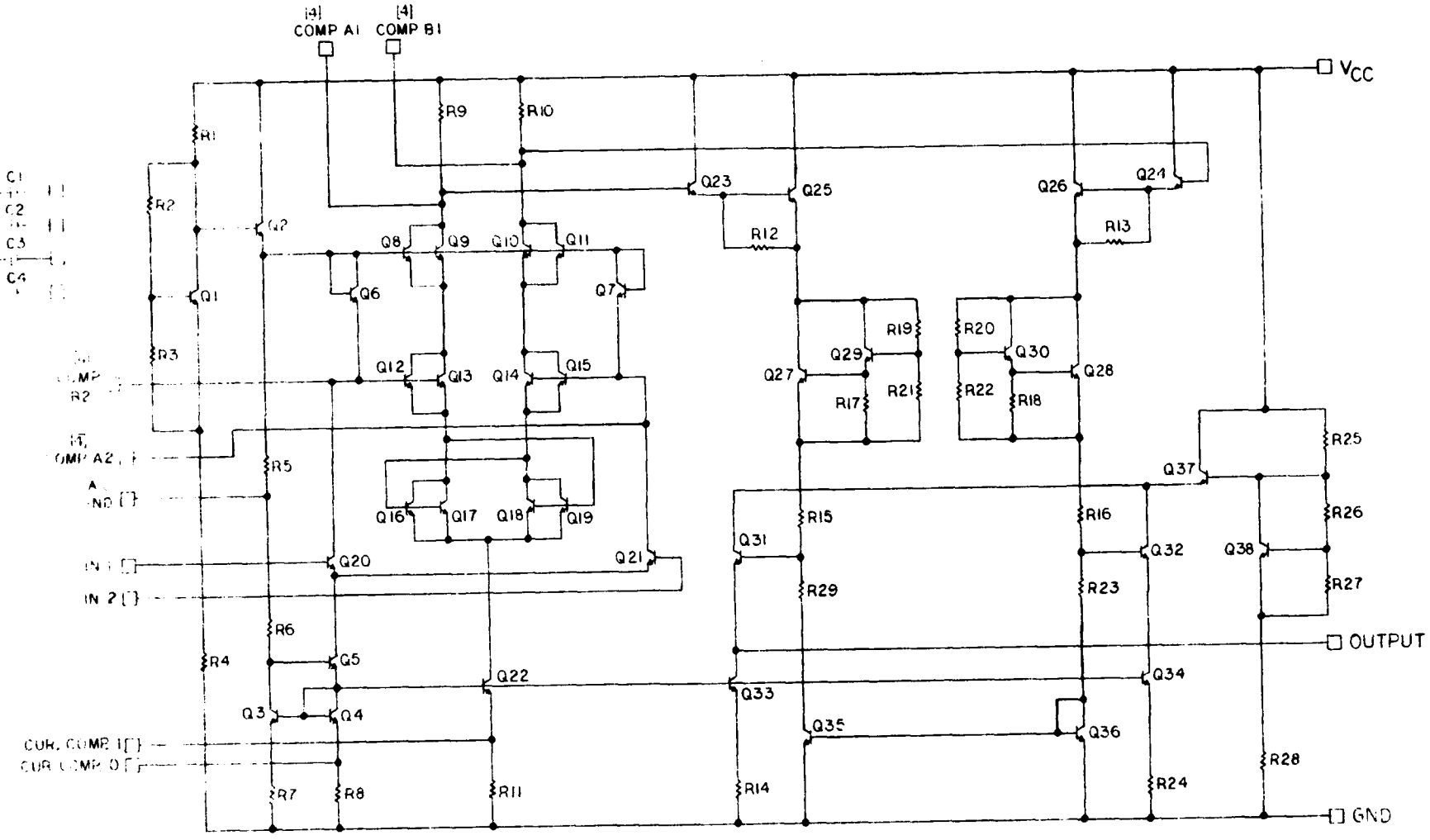
Transistor Q_1

CJC	= .02 pf	BF	= 60
CJE	= .08 pf	DELAY	= 25 ps
RB	= 160Ω	TF	= 24 ps
RE	= 2Ω	IK	= 8 mA
RC	= 120Ω	IS	= 2×10^{-16} A
VA	= 15 volts		

AD-A082 664 TRW DEFENSE AND SPACE SYSTEMS GROUP REDONDO BEACH CA --ETC F/G 9/5
HIGH FREQUENCY ANALOG LSI DEVELOPMENT.(U)
NOV 79 C A WEST, J CHOMA N00123-77-C-1045
UNCLASSIFIED TRW-30491-6014-RU-00 NOSC-TR-517 NL




1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
MICROCOPY RESOLUTION TEST CHART



RESISTOR VALUES ARE IN OHMS AT 200 OPS.

R1=500	R8=2.29K	R23=1.3K
R2=3.85K	R9,10=2K	R25=1.05K
R3=715	R12,13=530	R26=1.6K
R4=1.47K	R14,24=655	R27=780
R5=1.58K	R15,16=180	R28=2.1K
R6=845	R17,18=1.26K	C1-4=1.5PF [4]
R7=390	R21,22=1.56K	
R11=610	R19,20=890	
	R29=400	

RFCS-1
OP AMP
(11)

APPROVED
C. 6/11/79
28. 11 JUNE 1979
6/19/79

NOTES:
1. ALL TRANSISTORS ARE 2T2L12W4.
2. V_{CC} = +12.0VDC
3. P_D = 247mw
[4] PAD IS 3 MILS IN DIAMETER, METAL 2 ONLY.

Figure (5.19). Operational Amplifier Schematic Diagram.

OUTPUT (4.7 volts) that balances with the common mode voltage at IN1-IN2. Transistor Q31 provides an emitter follower output voltage extracted from the double-to-single-ended converter defined by Q35 and Q36. Transistor Q32 precludes an excessive imbalance on both sides of the level shifter and finally, Q37 and Q38 supply a stabilized bias for the emitter follower output.

Frequency compensation aimed toward ensuring at least 25° phase margin is implemented by connecting a capacitor between COMP A1 and COMP A2 and also, a capacitor is connected between COMP B1 and COMP B2. This interconnection gives rise to classical lag-lead compensation. The capacitors are available for bonding on chip as C1 through C4. Although 1.2 pF is deemed to be acceptable susceptive compensation, provisions have been made to incorporate more optimal values through appropriate series or parallel connection of the four capacitors embedded on chip.

The use of SPICE-2 leads to the conservative estimate of 77 dB of open loop gain, with 25°C phase margin and a unity gain frequency of 1.25 GHz. The model parameters are listed below.

BF = 65
IS = 2E-16 AMPS
RB (INTERNAL) = 200 ohms
RB (EXTERNAL) = 30 ohms
RC (INTERNAL) = 70 ohms
RC (EXTERNAL) = 30 ohms
RE = 3 ohms
TF = 25 ps
CJE = 0.1 pF
VA = 15V
PE = 0.85V
ME = 0.5
CJC (INTERNAL) = 0.025 pF
CJC (EXTERNAL) = 0.15 pF

PC = 0.75V
MC = 0.33
IK = 11 mA

Figure (5.20) shows the interconnection diagram for proper op-amp utilization. Resistor R_B should be nominally equal to the Thevenin source resistance seen by the driven input terminal. The 50 KΩ potentiometer implements balance between OUTPUT and AC GND, the latter being AC grounded by the 1 μF capacitor. This capacitor can, however, be omitted, although high frequency feedthrough problems may be incurred in its absence. Resistor R is a 20K potentiometer used to adjust for maximum gain and zero low frequency phase angle between OUTPUT and differential input signals. Capacitor compensation terminals are not shown since frequency compensation is effected by means of internal bonding.

5.5 Voltage Controlled Oscillator (VCO)

The VCO design uses one general purpose circuit to span center frequencies in the range of 100 MHz to 2 GHz. Stable oscillations at frequencies in excess of 3 GHz are theoretically possible, but detailed simulations have been completed only at 100 MHz, 1 GHz and 2 GHz. The actual center frequency is adjusted by a change of component values only. The input port is terminated externally to the chip by a series varactor-inductor combination or by a varactor terminated transmission line. The choice is generally determined by considerations of size, Q, and realizability. Generally, the varactor terminated transmission line is optimal above 1 GHz.

5.5.1 Circuit Description

Figures (5.21) through (5.23) depict schematic diagrams for VCO's designed for 2 GHz, 1 GHz and 100 MHz operation, respectively. Transistor Q1 in each diagram, along with its associated passive components, is used to generate a nonlinear negative resistance present at the input port. When the input port is properly terminated, oscillations occur at the

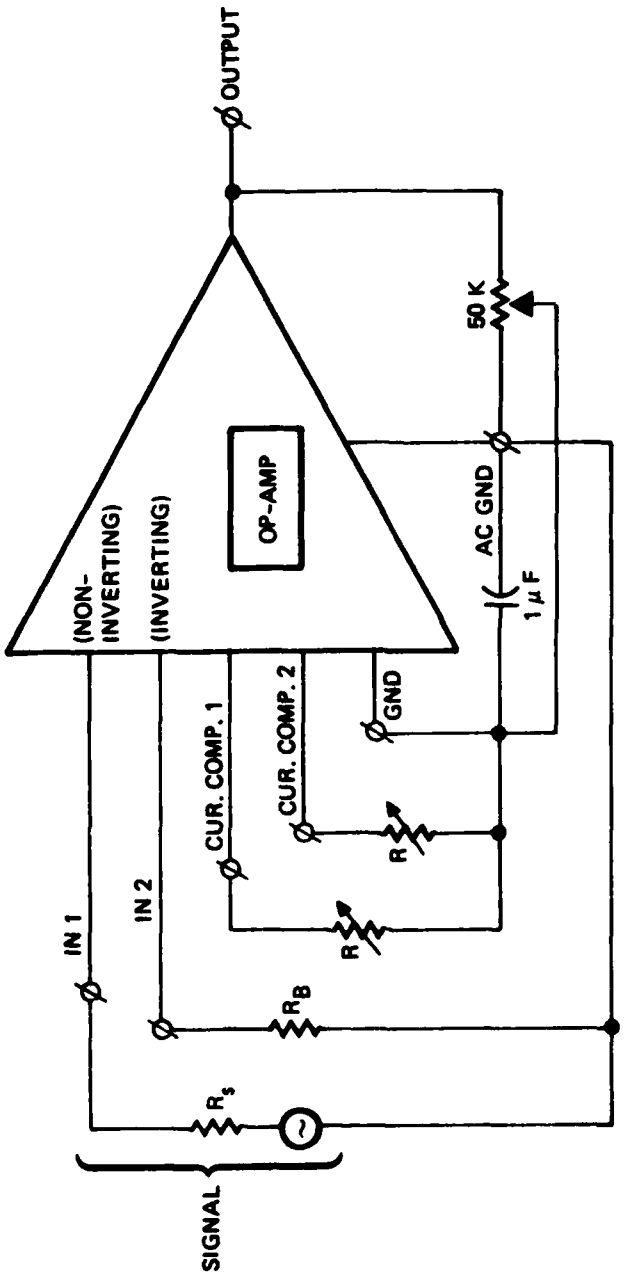
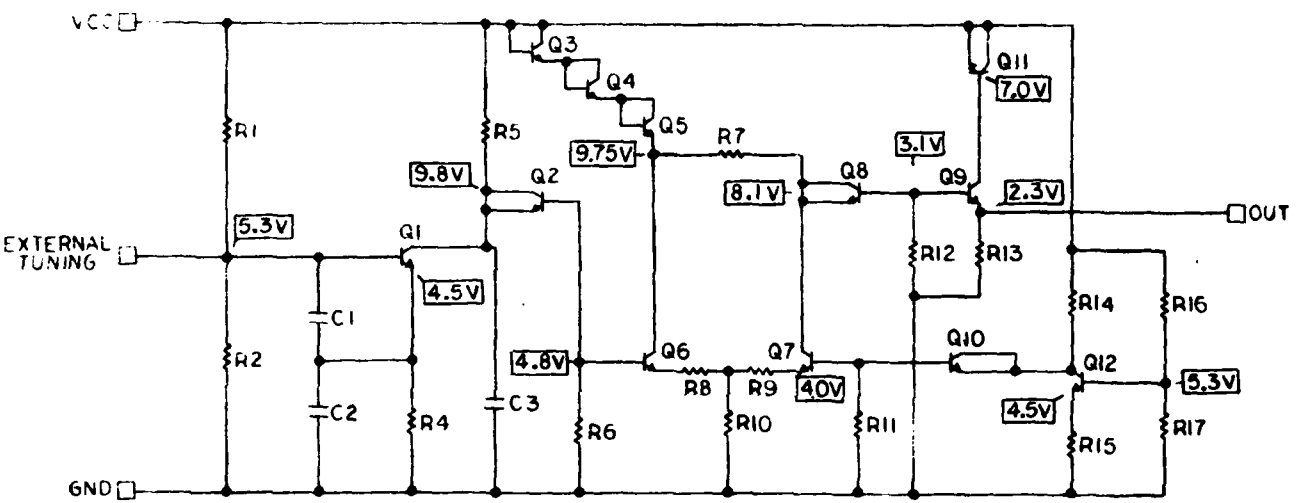


Figure (5.20). Typical Interconnection Diagram of Op-Amp.



RESISTOR VALUES ARE IN OHMS AT 200 OPS.

R1,16=6.5K
R2,17=5.3K
R4,15=1.5K
R5,14=500
R6,11=3.3K
R7,13=700
R3 NOT USED
R8,9=50
R10=2.0K
R12=2.2K
C1,2=0.2PF
C3=0.5PF

RFCS-1
VCO-2.0
④

DEVICE TYPES
Q1,9,11,12=2T2LI7W3
Q2,8,10=2TILI7W3
Q3,4,5=2T2LI2W3
Q6,7=2TILI2W3

NOTES:
1. Q2,8,10,11 ARE 5V ZENER DIODES.
2. C2=0.08PF PLUS 0.12PF PARASITIC OF C1.
3. VCC=+12VDC
4. P_D=200 MW

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29 MAY 1979

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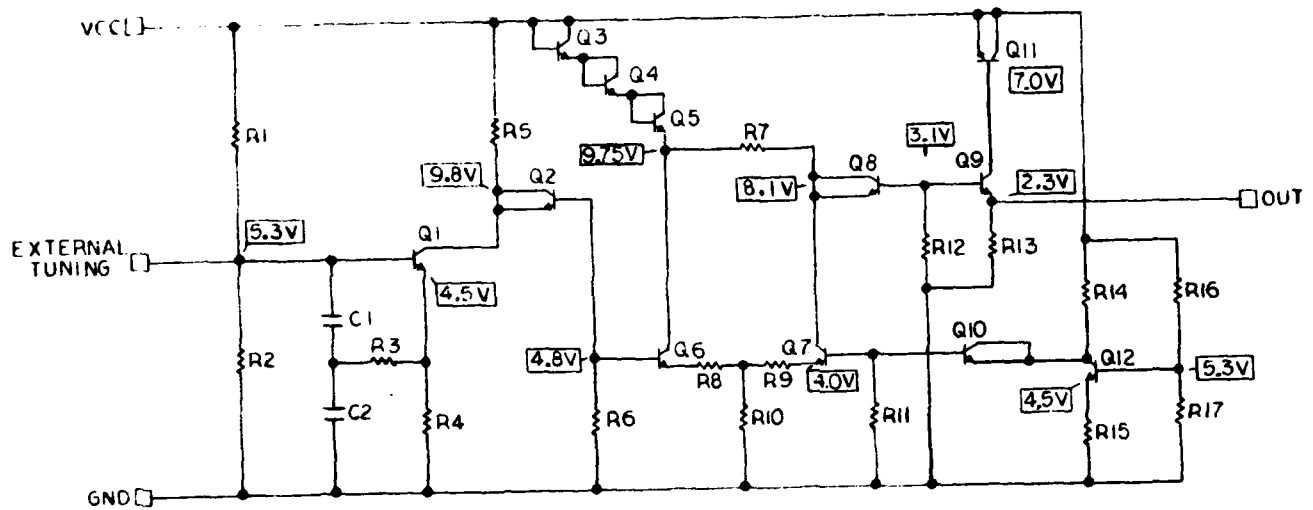
Figure (5.21). Schematic Diagram of 2 GHz VCO.



RESISTOR VALUES ARE IN OHMS AT 200 OPS.

R1,16=6.5K
R2,17=5.3K
R3=100
R4,15=1.5K
R5,14=500
R6,11=3.3K
R7,13=700
R8,9=330
R10=1.8K
R12=2.2K
C1,2=0.3PF

RFCS-1
VCO-1.0
③

DEVICE TYPES
Q1,9,11,12=2T2L17W3
Q2,8,10=2TIL17W3
Q3,4,5=2T2L12W3
Q6,7=2TIL12W3

NOTES:
1. Q2,8,10,11 ARE 5V ZENER DIODES.
2. C2=.12PF PLUS .18PF PARASITIC OF C1.
3. VCC=+12 VDC
4. P_D=200 MW.

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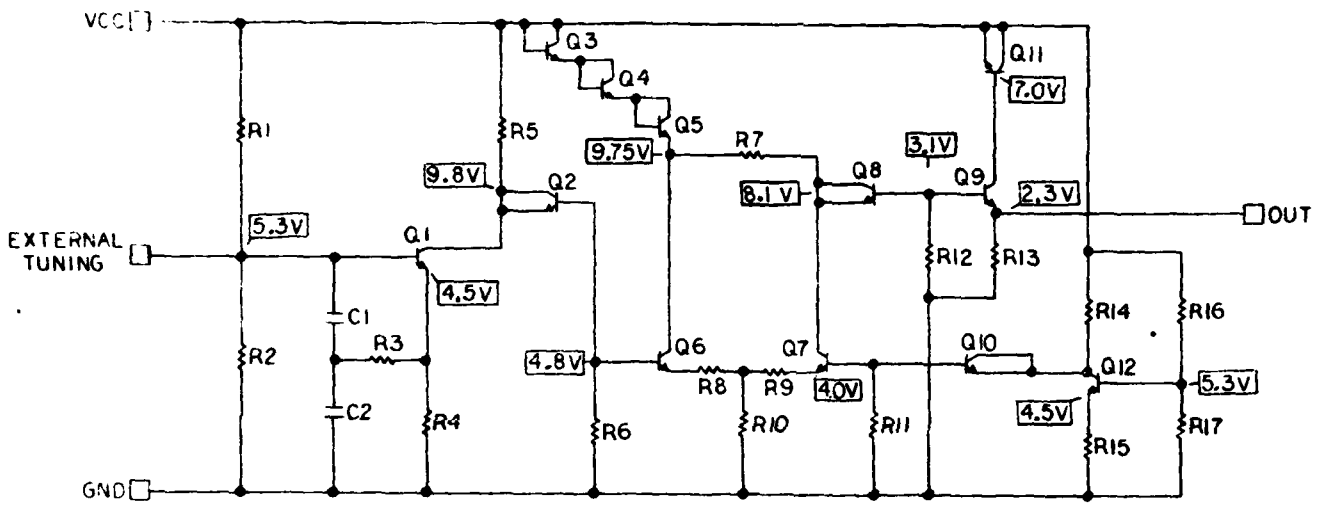
Figure (5.22). Schematic Diagram of 1 GHz VCO.



RFCS-1
VCO-0.1
②

RESISTOR VALUES ARE IN OHMS AT 200 OPS,

R1,16=6.5K	R7,13=700
R2,17=5.3K	R8,9=900
R3=510	R10=1.55K
R4,15=1.5K	R12=2.2K
R5,14=500	
R6,11=3.3K	C1,2=3.4PF

DEVICE TYPES
Q1,9,11,12=2T2L17W3
Q2,8,10=2TIL17W3
Q3,4,5=2T2L12W3
Q6,7=2TIL12W3

NOTES:
1. Q2,8,10,11 ARE 5V ZENER DIODES.
2. C2=1.4PF PLUS 2.0PF PARASITIC OF C1.
3. VCC+12VDC
4. P_D=200 MW

Edward S. Meaux 5-11-79
Design Mgr 5-11-79
Proj Engineer 11 MAY 79

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Figure (5.23). Schematic Diagram of 100 MHz VCO.

collector of Q1. The Q3-Q4 differential pair is biased by Q1 and Q2. The differential pair presents a high input impedance to the collector circuit at Q1 and provides isolation to same from the external output load. Transistor Q5 actively transforms the impedance present at the collector of Q4 to about 50Ω with some inductive reactance at the output. An external capacitor in series with the chip output serves as a DC block and cancels the output inductive reactance, thereby providing a 50Ω match.

5.5.1 Circuit Analysis

According to Kurakawa's theory [22], an oscillator can be thought of as a nonlinear impedance with a negative real part in series with a passive linear tuning circuit as depicted in figure (5.24). The oscillation frequency, ω, and RF current amplitude, A, are gleaned from a solution of

$$\overline{Z}(\omega) - \overline{Z}(A) = 0. \qquad (5\text{-}40)$$

It is instructive to have at least a qualitative understanding of how Q1 with its peripheral components generates the device impedance with its negative real part. To this end, a simplified hybrid-pi common emitter circuit is modeled in figure (5.25) and a negative resistance is shown to exist at the base.

With an input current of unit magnitude and zero phase, V_{in} is numerically equivalent to Z_{in}. In order to have a negative real part, it is necessary to show that the phase of V_{in} lies between +90° and +270°. Since the conductance due to C_π is much greater than that due to r_π (25 times greater in 2 Gc design), voltage V_π lags the RF base current by nearly 90°. This voltage creates a larger collector current, $g_m V_\pi$ which accounts for the majority of the current flowing through the parallel combination of R_e and C_e. Since most of this conductance is capacitive, V_e has an additional lag of nearly 90°, and its total lag therefore approaches 180°. Since the impedance of the parallel C_e and

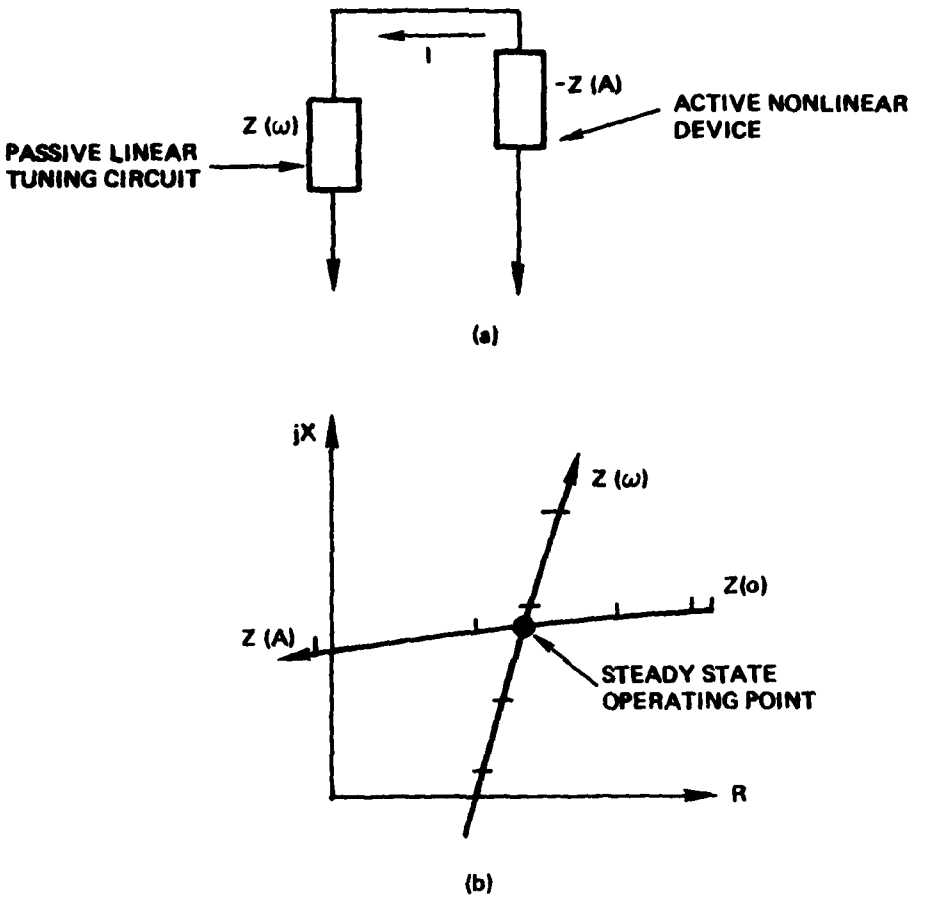

Figure (5.24). (a) Symbolic Representation of Negative Resistance Oscillator.

(b) Tuning Impedance and Active Device Impedance Loci, Z and $\bar{Z}$, as Functions of Frequency and Current, Respectively.

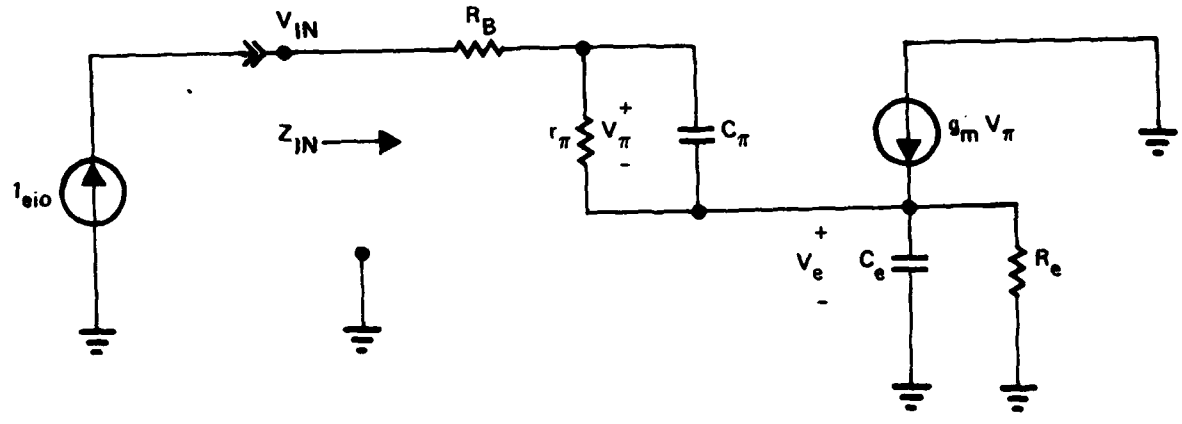

Figure (5.25). Simplified Small-Signal Model of Common Emitter Amplifier [Q1 in Figure (5.21)].

R_e combination is much larger (by a factor of 13 for the 2 GHz design) than that of the r_π, C_π combination and since the emitter current flowing through C_e and R_e is greater than the base current flowing through r_π and C_π, the voltage V_e is much greater than V_π and nearly equal to V_{in}. Therefore, V_{in} has a phase angle approaching 180° and Z_{in} has a negative real part.

By writing Kirchoff's current equations for the circuit in figure (5.25), the following expressions for R_{in} can be derived.

$$R_{in} \approx R_B + \frac{g_\pi}{(\omega C_\pi)^2} + \frac{G_e}{(\omega C_e)^2} - \frac{g_m}{\left[\omega^2 C_e C_\pi + \left(\frac{g_\pi}{C_e C_\pi^2} + \frac{G_e}{C_e^2 C_\pi}\right)^2\right]}, \quad (5\text{-}41)$$

provided

$$\left.\begin{aligned} G_e g_\pi &<< \omega^2 C_e C_\pi \\ G_e^2 &<< (\omega C_e)^2 \\ g_\pi^2 &<< (\omega C_\pi)^2 \end{aligned}\right\}. \quad (5\text{-}42)$$

Equation (5-42) is generally invalid for frequencies substantially lower than the oscillation frequency. Therefore, in the neighborhood of the oscillation frequency,

$$R_{in} \quad R_B - \frac{g_m}{\omega C_e C_\pi}. \quad (5\text{-}43)$$

Equations (5-41) and (5-43) show that R_{in} decreases linearly with g_m. The large-signal transconductance, $g_m(x)$, is expressible as

$$g_m(x) = g_{mo}[x2I_1(x)/I_o(x)], \quad (5\text{-}44)$$

where I_1 and I_o are modified first and zeroth order Bessel functions, g_{mo} is the small signal transconductance and x is the peak RF voltage across the base-emitter junction normalized to kT/q = 26 mV [23]. Since $g_m(x)$ monotonically decreases from its small signal value with increasing base emitter drive level, x, the magnitude of the negative input resistance is a maximum for small signals and monotonically decreases with increasing drive level. This relationship is commensurate with the device line characteristic shown in figure (5.24) and it bounds the steady state amplitude of oscillation A.

Because of large DC emitter degeneration in Q1, Q2 and Q5, the bias stability of these devices is not a problem. It must be shown, however, that the Q3-Q4 differential amplifier maintains balanced operational dynamics. If a factor of two variation in collector bias current of Q4 is permitted, one can derive bounds on the voltage imbalances that can be tolerated at the bases of the Q3-Q4 pair. The low frequency transconductance for the single-ended output differential pair is

$$G_M = \frac{\beta}{2(R_e + r_\pi + \beta R_e)} . \qquad (5\text{-}45)$$

Substituting the appropriate values into (5-45) for the three designs leads to explication of tolerable differential voltage imbalances. These imbalances, which are caused by zener voltage and bias resistor mismatches in the Q_1 and Q_2 circuitry, are given in Table (5.8).

Table (5.9) lists projected performance specifications for each of the three VCO units.

5.6 RF Switch

The RF switch fabricated in RFCS-1 is a single-pole, four-throw (SP4T) structure designed to provide 70 dB of isolation between the unselected inputs and the selected input, as measured at switch output. A block diagram of the switch is provided in figure (5.26), and cognate

TABLE (5.8)

TOLERABLE VOLTAGE IMBALANCE IN VCO

	100 MHz	1 GHz	2 GHz
Tolerable Differential Voltage Imbalance	375 mV	128 mV	50 mV

TABLE (5.9)

VCO PERFORMANCE SPECIFICATIONS (SIMULATED)

A. 2 GHz Design

Pulling Range:	1943 MHz to 2115 MHz, or Δf = 8.6%
Temperature Coefficient:	-330 PPM/°C
Dissipation:	200 mW at 12V
Power Output Into 50Ω:	-12.7 dBm at 27°C -14.4 dBm at 70°C -11.9 dBm at 5°C

B. 1 GHz Design

Pulling Range:	969 MHz to 1065 MHz, or Δf = 9.6%
Temperature Coefficient:	-140 PPM/°C
Dissipation:	200 mW at 12V
Power Output Into 50Ω:	5°C - 9.7 dBm 25°C - 9.7 dBm 70°C - 11.0 dBm

C. 100 MHz Design

Pulling Range:	97.4 to 106.4 MHz, or Δf = 9.04%
Temperature Coefficient:	-73 PPM/°C
Dissipation:	200 mW at 12V
Power Output Into 50Ω:	-12 dBm at 25°C

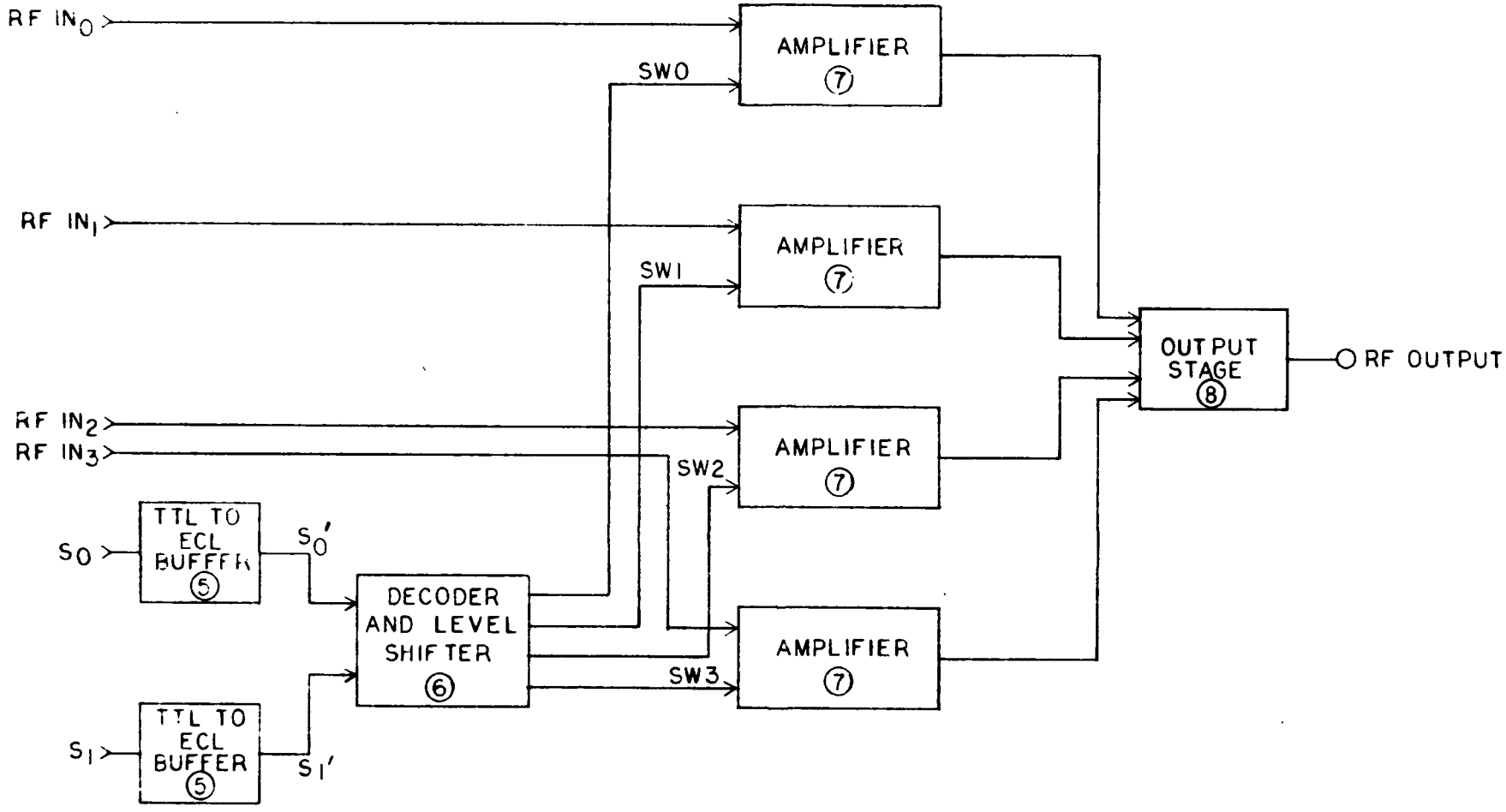

Figure (5.26). RF SWITCH BLOCK DIAGRAM

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Dennis Cocco 6-19-79
Dick Carlson 19 JUNE 1979

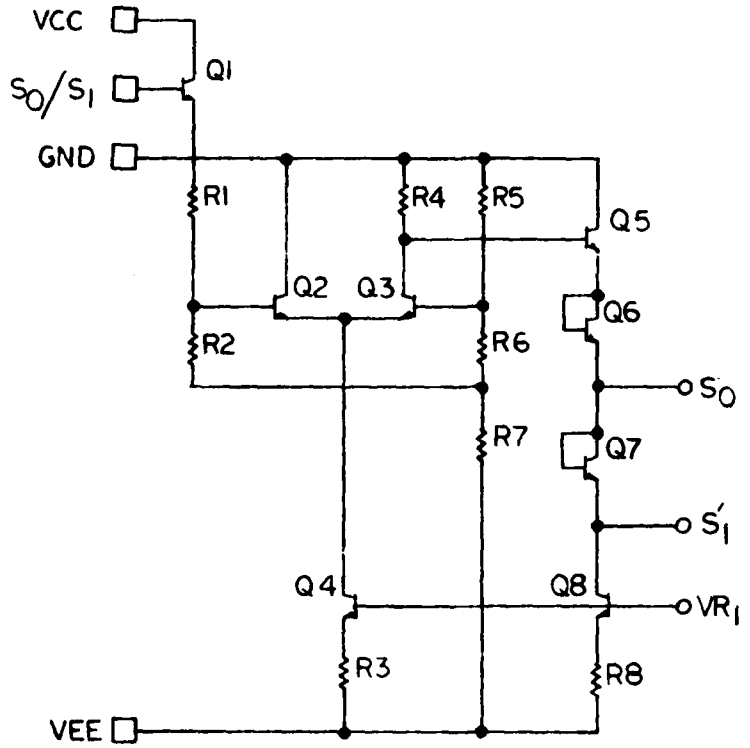
DRWN 6-14-79 CS

circuit diagrams appear in figures (5.27) through (5.30). The projected performance specifications are tabularized in Table (5.10).

A number of features are included in the RF switch design to satisfy the stipulated isolation requirement. To avoid coupling through power supply or ground impedances, all critical circuitry is differential in nature. The input signal derives from a single-ended termination and accordingly, the complimentary side of each differential input is grounded at the ground terminal of the transmission line supplying that input. Also, since the selected channel is designed to have gain, less attenuation is required in unselected channels.

Power supplies are ± 5 volts. The select levels accept TTL levels between 0 and +5 volts.

With reference to the block diagram and appropriate schematic diagrams, the selected signal in the ON state is seen to be amplified by two differential common-emitter/common base cascode stages. The first stage includes active peaking for broadbanding purposes. The gain is stabilized by emitter degeneration resistors in the selected channel. The second common base stage serves to combine all channels, in addition to enhancing circuit gain. In the OFF state, isolation from input-to-output is dominantly achieved by virtue of the two common base stages, which are reverse biased when they are not selected. All inputs and the output are capacitively coupled.



RESISTOR VALUES ARE IN OHMS AT 200 OPS

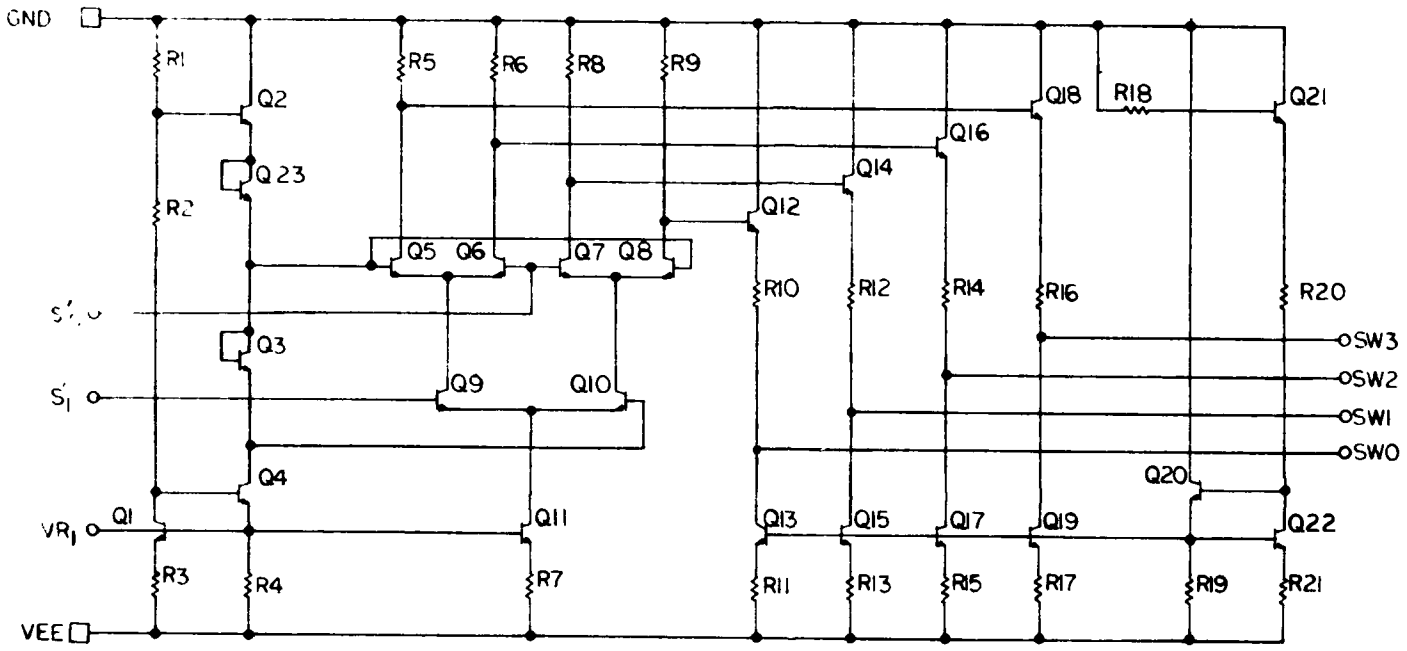
1. R1=2.4K
2. R2,R6=1.2K
3. R3,R7,R8=1K
4. R4=2K
5. R5=1.8K

NOTES:

1. VEE=-5.0VDC
2. ALL TRANSISTORS ARE 2TIL12W4
3. VCC=+5.0 VDC
4. P_D = 20mw

DRAWN BY Jerry Kalk 4-27-79
APPROVED [illegible] 5-7-79
Leo Enders 7 MAY '79
REVISED 5-7-79 JK

Figure (5.27). TTL-to-ECL Buffer



RFCS-1

RESISTOR VALUES ARE IN OHMS AT 200 OPS.

1. R1,R3=800
2. R2=5.28K
3. R4,R19 = 24K
4. R5,R6,R8,R9,R18=1200
5. R7=600
6. R10,R12,R14,R16 = 4.66K
7. R11,R13,R15,R17,R21 = 475
8. R20=5.0K

NOTES:
1. VEE=-5.0 VDC
2. ALL TRANSISTORS ARE 2TIL12W4
3. P_D=23.0mw
4.

S_0	S_1	SELECT
0	0	SW0
0	1	SW3
1	0	SW1
1	1	SW2

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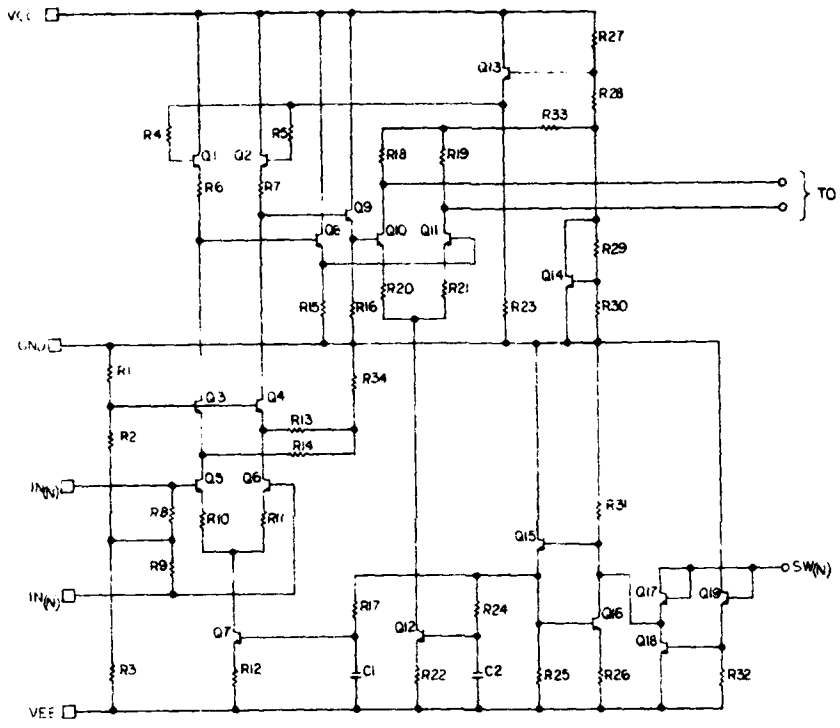
APPROVED. [illegible] 5-8-79
Bio Codes 7MAY'79
REVISED - 18 JUNE '79 CIS

Figure (5.28). Decoder and Level Shifter.



RFCS-1

RESISTOR VALUES IN OHMS AT 200 OPS

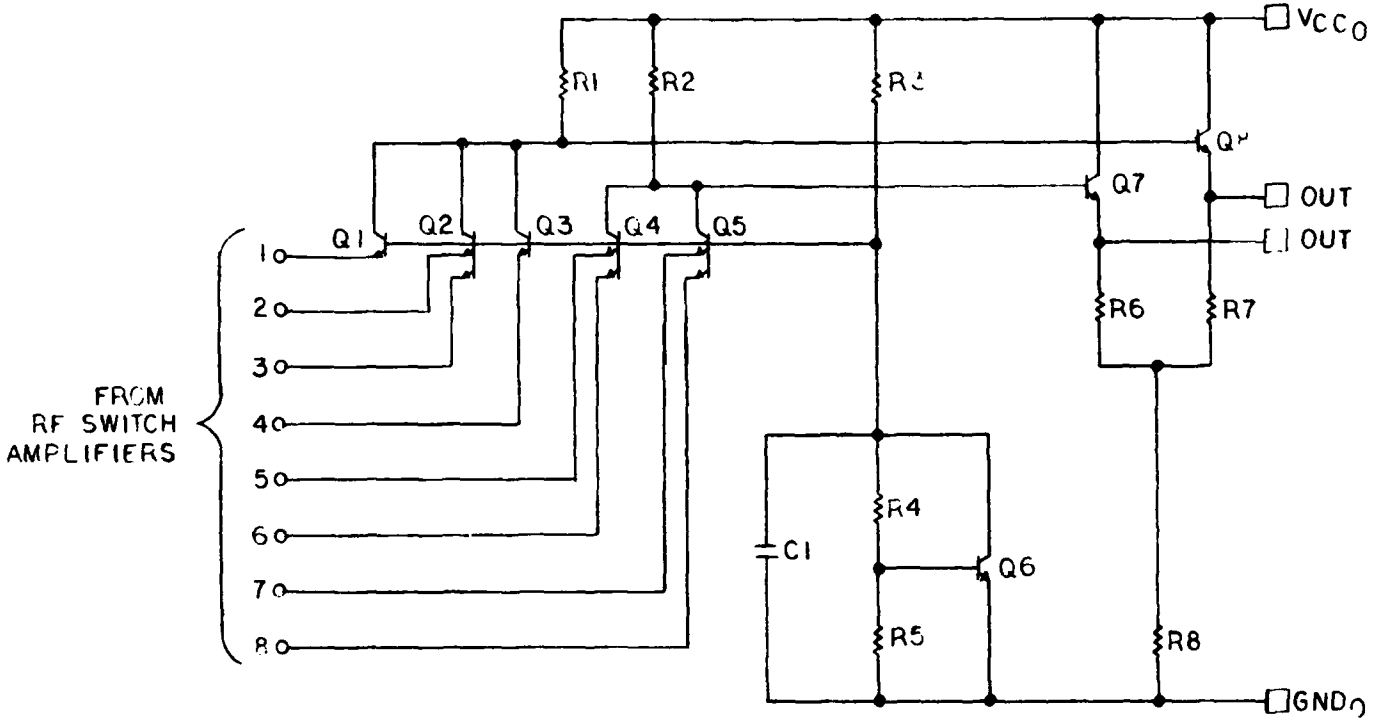
1. R1, R17, R24 = 400
2. R2 = 56K
3. R3 = 35K
4. R4, R5 = 1200
5. R6, R7 = 250
6. R8, R9, R15, R16, R13, R14 = 1K
7. R10, R11, R20, R21 = 30
8. R12, R22 = 250
9. R18, R19, R30 = .5K
10. R23 = 4K
11. R25 = 500
12. R26 = 900
13. R27 = 13K
14. R28 = 350
15. R29 = 4.2K
16. R31 = 5.6 EK
17. R32 = 16K
18. R33, R34 = 50K
19. C1, C2 = 2.4 pf

NOTES

1. VEE = -5.0 VDC
2. ALL TRANSISTORS ARE 2T1L12W4
3. CAPACITORS ARE BURIED LAYER TO ISOLATION DIODES.
4. VCC = 5.0 VDC
5. INPUT PADS ARE 4 MILS IN DIAMETER.
6. P_D = 57.6 mw

DRAWN BY Jerry Kalk 5-4-79
APPROVED [illegible] 4 MAY 1979

Figure (5.29). RF Switch Amplifier Schematic.



RESISTOR VALUES ARE IN OHMS AT 200 OPS

R1,2=200
R3=1.65K
R4=4.2K
R5,8=1.5K
R6,7=1K
C1=2.0 PF

RFCS-1

NOTES:

1. ALL TRANSISTORS ARE 2TIL12W4
2. V_{CCO}=5.0+VDC
3. CAPACITOR IS BURIED LAYER TO ISOLATION DIODE.
4. OUTPUT PADS ARE 4 MILS IN DIAMETER.
5. P_D=19.6 mw

APPROVED
Dennis Cocco 6/11/79
Dio Codero 8 JUNE 1979
REDRWN - C.I.S 8 JUNE 79

Figure (5.30). RF Switch Output Stage.

TABLE (5.10)

RF SWITCH

PERFORMANCE SPECIFICATIONS (SIMULATED)

Supply Voltage:	$\pm$5V
Power Dissipation:	320 mW
Select Command:	TTL compatible (2 bits)
Selected Channel Voltage Gain:	15 dB
Unselected Channel Voltage Attenuation:	>55 dB
Channel Bandwidth (3 dB):	600 MHz
Channel Differential Input Impedance:	>200Ω over channel bandwidth
Channel Differential Output Impedance:	<100Ω over channel bandwidth
RF Input Signal Level:	<20 mV peak (differential)
Switching Time:	<20 ns

NOTES:

1) Circuit package has 6 V_{CC}, 5 V_{EE}, and 5 ground connections to minimize crosstalk between channels.

2) IF input signal is single-ended, the complimentary side of each differential input should be grounded at the ground terminal of the transmission line supplying that input.

6.0 GPS CIRCUIT CHARACTERIZATION

6.1 General Discussion

The challenges associated with the characterization of the GPS circuits fell into two basic categories: those derived from the difficulties in making meaningful measurements at frequencies above 100 MHz, and those that stemmed from the uncertainties of LSI circuit production yield. The usual procedure of screening circuits by wafer probe testing before detailed characterization was subverted by the lack of proven high frequency probe testing techniques and by the lack of data relating easily measurable low frequency parameters with the high frequency performance of these circuits.

The approach used to obtain the data presented in this report was to bond random samples of each circuit type in standard 14-lead flat packages and to construct test fixtures so as to facilitate easy insertion and removal of the packaged circuits without unduly compromising high frequency measurement integrity. This allowed the rapid screening of test devices at design nominal frequencies. Appropriate calibration elements (short, open, through, and load) were also bonded in the 14 lead packages to provide reference data for the evaluation of fixture performance and to permit the extraction of device performance data from raw measurements.

The test fixtures were fabricated with the following basic guidelines.

a. All fixtures were made as small as feasible; most were constructed in a 5" x 2" x 3/4" box (MODPAK 7124-4).

b. All high frequency inputs and outputs were made via SMA connectors with .086 semi-rigid coax leading to the test socket pads.

c. The test sockets consisted of modified AUGAT type 8075-1G3 fixtures (package leads clamped to coplanar pads) mounted on double-sided copper clad boards.

d. All external bias, decoupling, and bypass circuit elements were placed as close to the test socket pads as possible.

6.2 Test Results

6.2.1 Summary

Samples of the GPS system and four subsystem test circuit chips taken from four wafers were bonded in 14-lead flat packages. The package devices of each type were screened at the nominal conditions determined from system design. Several representative or optimal devices were then selected for detailed characterization.

The quantities of each device type tested and characterized from each of the sampled wafers are listed in table (6.1). A summary of the general performance parameter measurement results for each circuit type is given in table (6.2).

6.2.2 Analog Multiplier

The test packages for the GPS analog multiplier were configured as shown in figure (6.1). The packaged devices were characterized using the circuit shown in figure (6.2), which allowed the three-input multiplier to be tested as a two-input multiplier by providing a static bias to the CODE input. A total of twenty-four devices were screened for performance at the design nominal conditions and five devices were then selected for more detailed characterizations.

The analog multiplier gain factor k, defined by the linear relationship $P_{IF} = kP_{LO}P_{RF}$, is shown for one representative device at GPS nominal conditions in figure (6.3). The gain factor for the same device as a function of varying RF input frequency, with the LO input frequency adjusted to yield a constant IF output frequency

TABLE (6.1)

GPS TEST SAMPLE SUMMARY

	WAFER* (GPS-1)		(GPS-1A)		
Circuit	1-6	1-8	2-14	3-19	Total
MULTIPLIER	2 (6)	1 (10)	1 (4)	1 (4)	5 (24)
IF AMPLIFIER	2 (6)	---	2 (4)	---	4 (10)
RF AMPLIFIER	1 (4)	---	2 (6)	2 (8)	5 (18)
LO BUFFER	---	---	2 (4)	2 (4)	4 (8)
SYSTEM	---	0 (2)	1 (6)	1 (6)	2 (14)

*sample from each wafer given as n (m);

where n = number of dice characterized,
and m = number of dice packaged.

TABLE (6.2)

GPS TEST RESULTS SUMMARY

Circuit	I_{CC} (V_{CC} = +12V)	I_{EE} (V_{EE} = -6V)	P_{DC}	Nominal Gain (frequency)	Maximum Gain (frequency)	N_{FIG} (frequency)
MULTIPLIER	7.8 mA	8.4 mA	144 mW	15 dB (1575 MHz)*	21.7 dB (475 MHz)*	-----
IF AMPLIFIER	14 mA	---	165 mW	19.0 dB (143 MHz)	29.6 dB (25 MHz)	15.7 dB (143 MHz)
RF AMPLIFIER	47 mA	---	566 mW	3.5 dB (1575 MHz)	30 dB (250 MHz)	13.1 dB (1575 MHz)
LO BUFFER	10 mA	9.5 mA	177 mW	0 dB (1432 MHz)	14.5 dB (80 MHz)	<26 dB (1432 MHz)
SYSTEM	126 mA	50 mA	1810 mW	17 dB (1575 MHz)*	55 dB (575 MHz)*	-----

*Gain factor k (= $P_{IF}/P_{LO}P_{RF}$) with f_{RF} tabulated; f_{IF} = 143 MHz, f_{LO} = f_{RF} - 143 MHz.

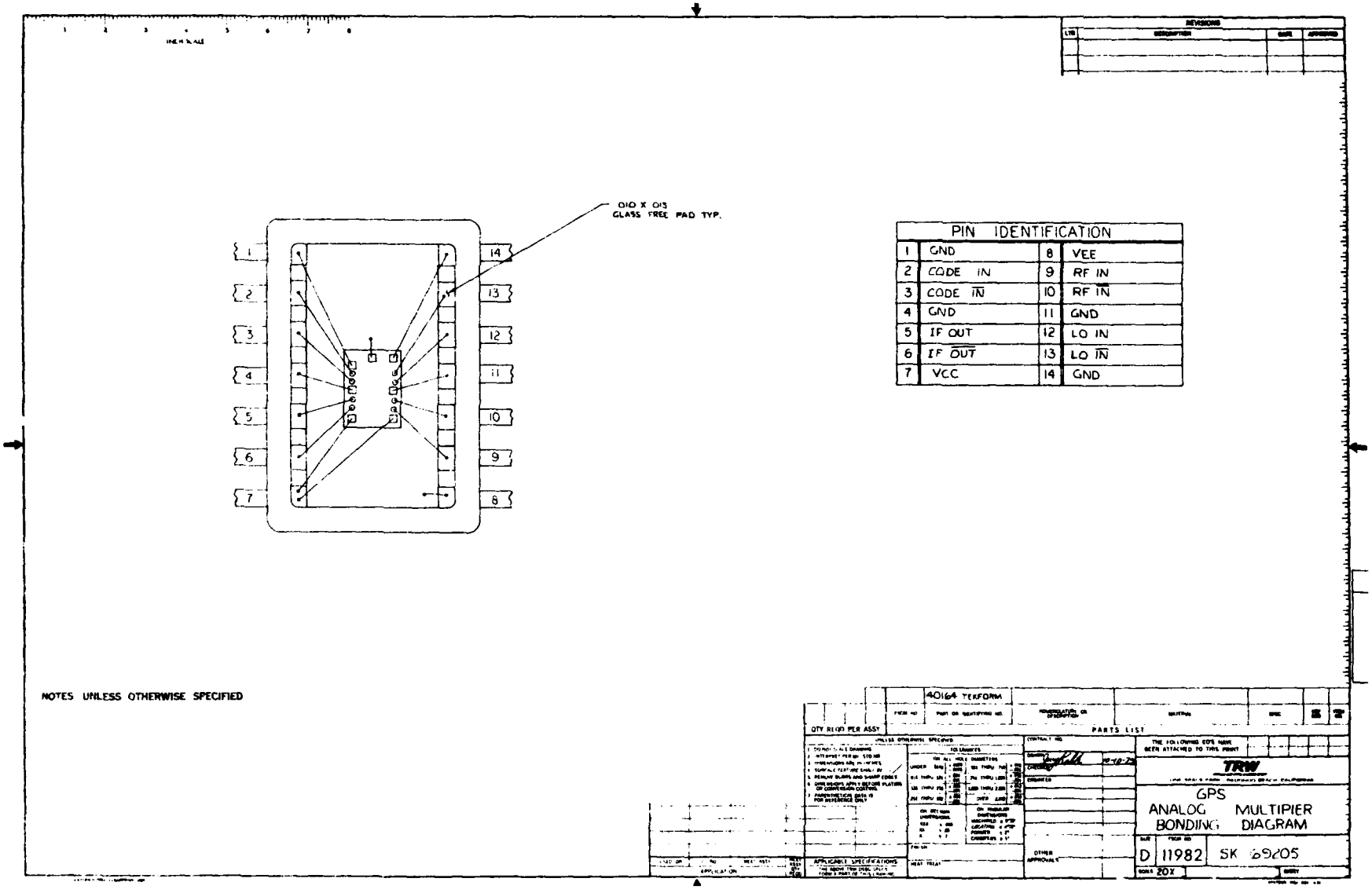
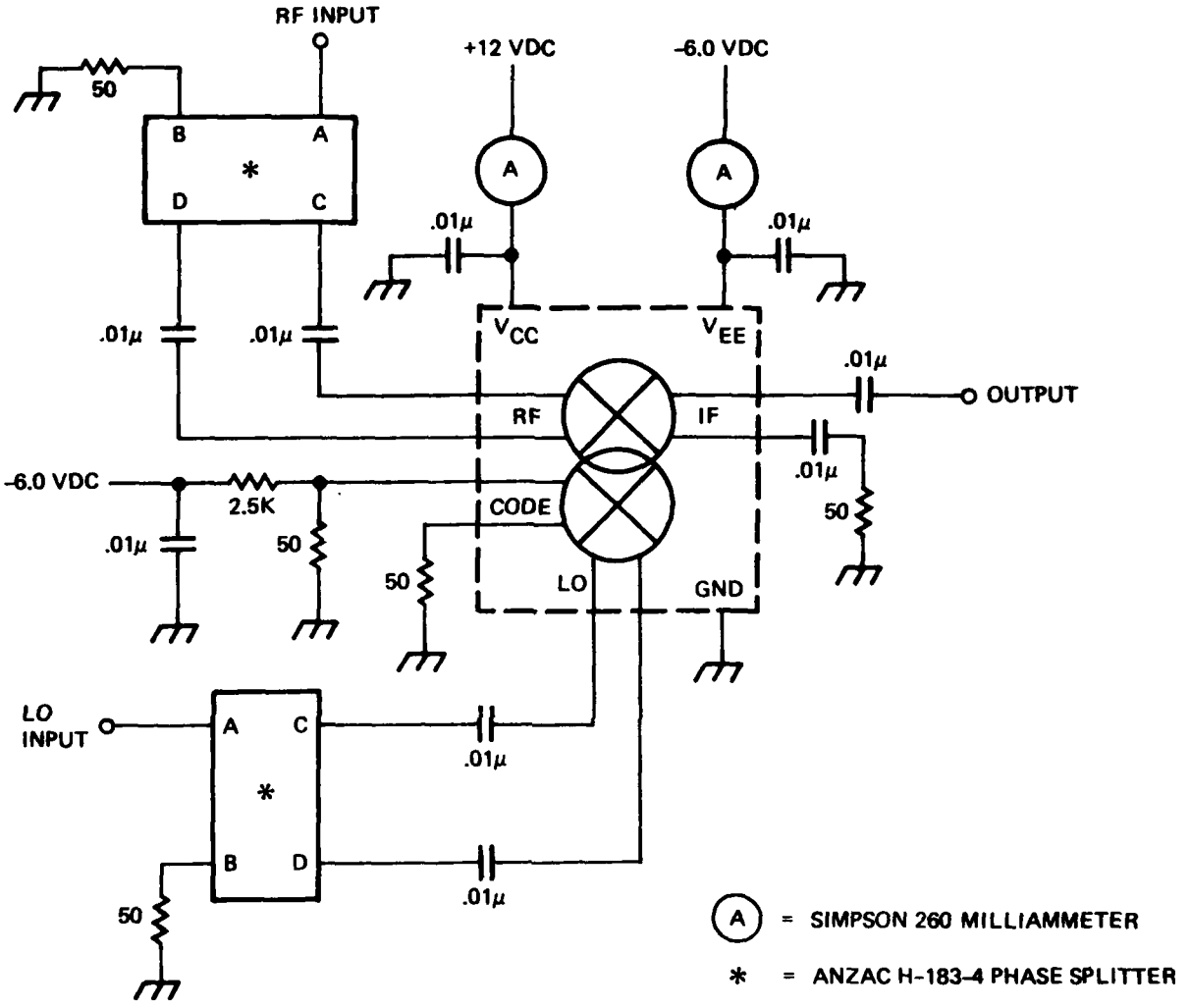


Figure (6.1). GPS Analog Multiplier Test Package Diagram.



NOTES:
1. OUTPUT MONITORED WITH (HP 141T/8555A/8552B) SPECTRUM ANALYSER.
2. RF INPUT SUPPLIED BY HP8660C/86603A OR HP612A SIGNAL GENERATOR.
3. LO INPUT SUPPLIED BY HP 8614A OR HP 8660C/86603A SIGNAL GENERATOR.

Figure (6.2). GPS Analog Multiplier Test Circuit.

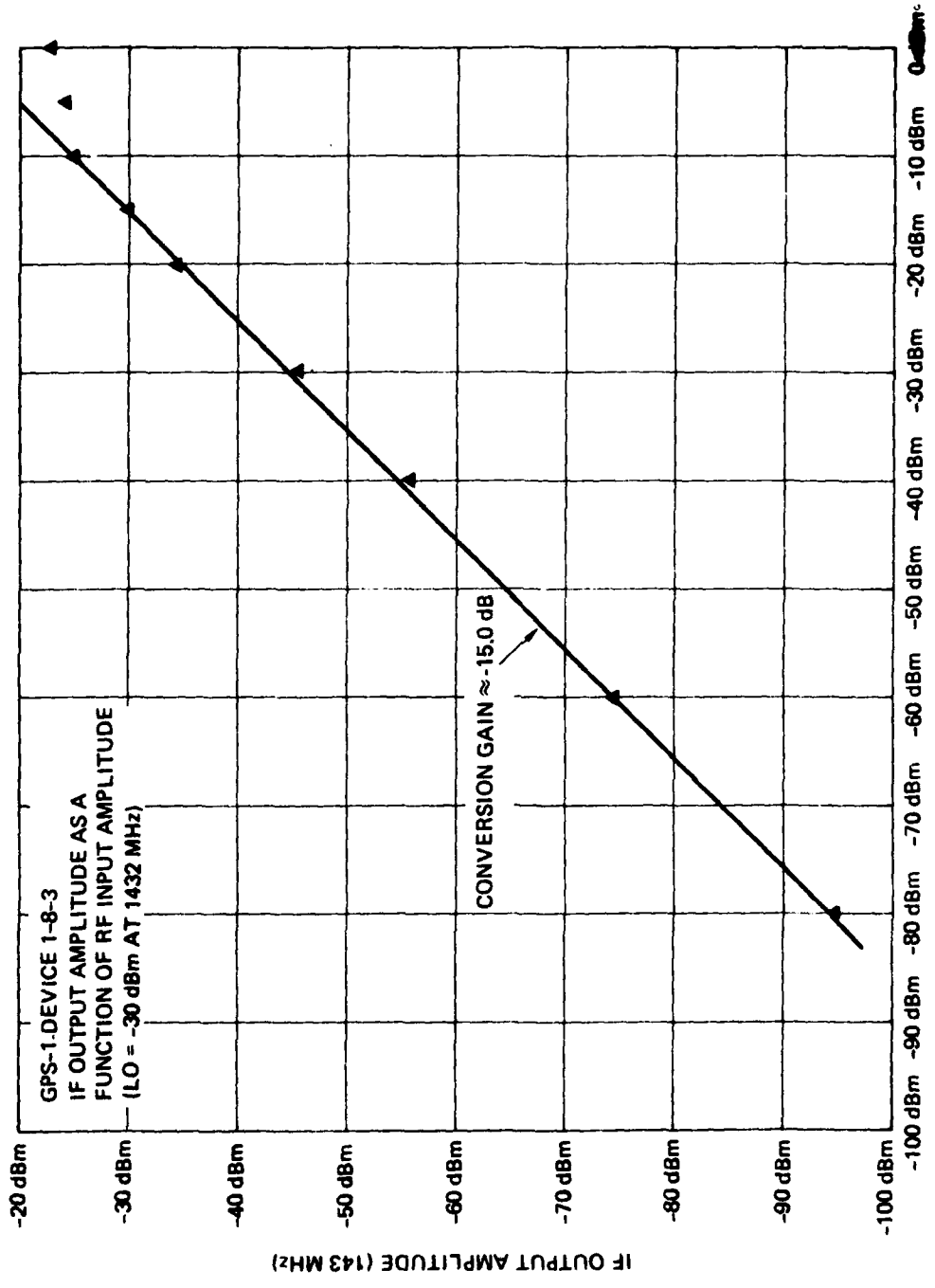


Figure (6.3). GPS Analog Multiplier Output Compression at 143 MHz.

of 143 MHz, is presented in figure (6.4). This data indicates a low frequency gain greater than 21 dB with a high frequency double pole roll-off breaking at about 1100 MHz. Also note that the data were obtained in two groups with nearly a week between tests; the observed scatter is thus indicative of the realizable measurement repeatability.

Figure (6.5) shows data for an up-conversion application of the multiplier, the measured IF output power graphed as a function of LO input power with RF input power held constant. In addition to data taken with the normal 50Ω IF output loads, data is also given for 100Ω IF output loads (accomplished by increasing the unused output termination and adding 50Ω in series with the spectrum analyzer and correcting the resulting measurements). Note that, for P_{LO} = -30 dBm (and P_{RF} = -30 dBm), the gain factor is 31 dB for the 50Ω loaded case and 38 dB for the 100Ω case.

6.2.3 IF Amplifier

The GPS IF Amplifier chips were packaged for testing as shown in figure (6.6). Four devices were selected for characterization from a total sample of ten packaged chips. All tests were made using the circuit configuration of figure (6.7).

IF Amplifier output power as a function of input power at the nominal operating frequency of 143 MHz is shown plotted for two devices in figure (6.8). Both devices exhibit 1 dB gain compression near 0 dBm output level. The variation of power gain at 143 MHz with increasing manual gain control (MGC) voltage is given in figure (6.9) for the two devices. Note that the gain of neither sample is affected until the MGC voltage exceeds 6.5V.

Figure (6.10) and (6.11) present the gain magnitude and phase for two IF amplifiers as a function of frequency. Although more low frequency data is necessary to define the flat gain band, a well-defined double pole roll-off beginning at 60 MHz dominates the plotted data. The low frequency phase data also shows the effects of 60 MHz double

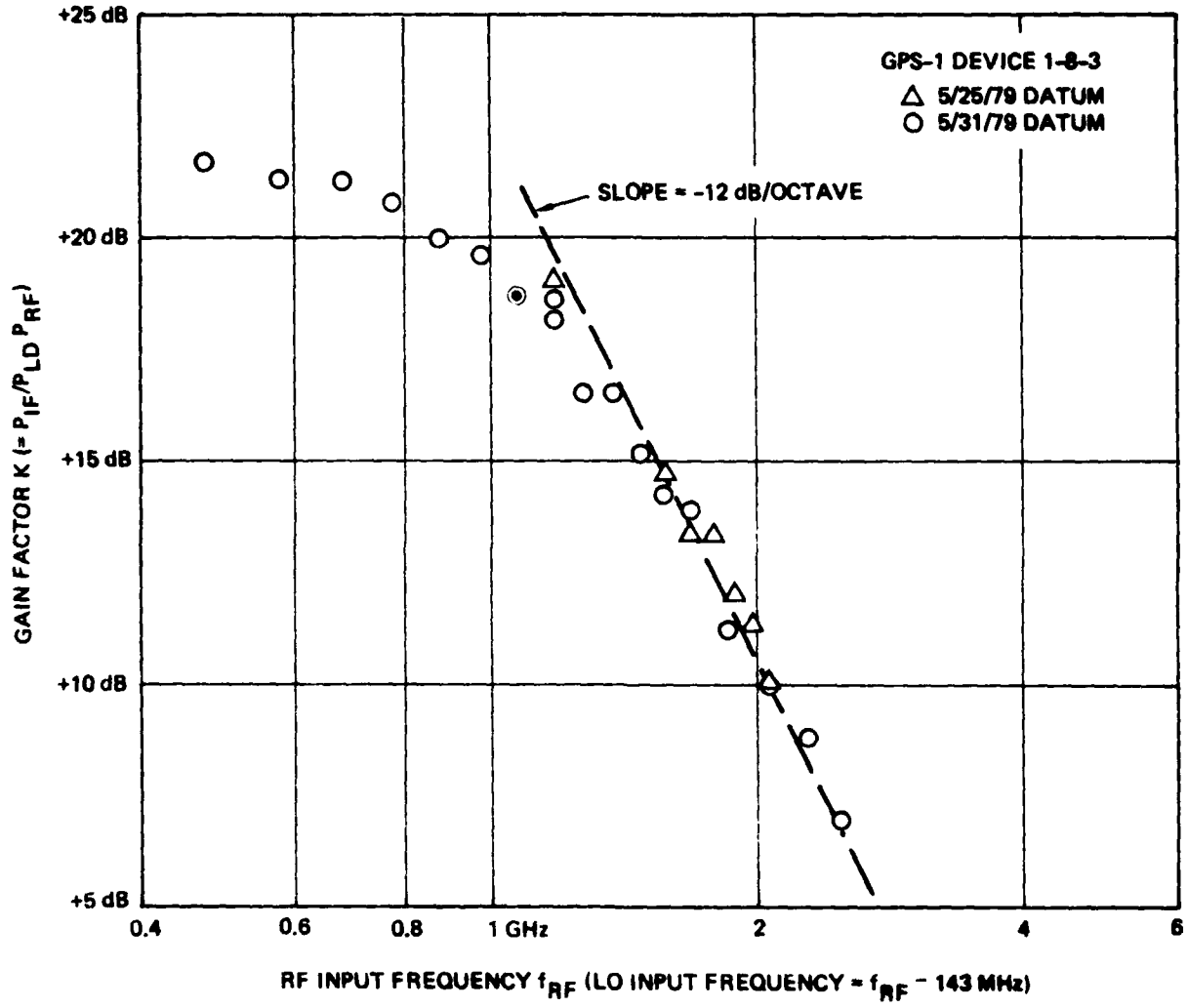


Figure (6.4). GPS Analog Multiplier Gain Factor as a Function of Input Frequency.

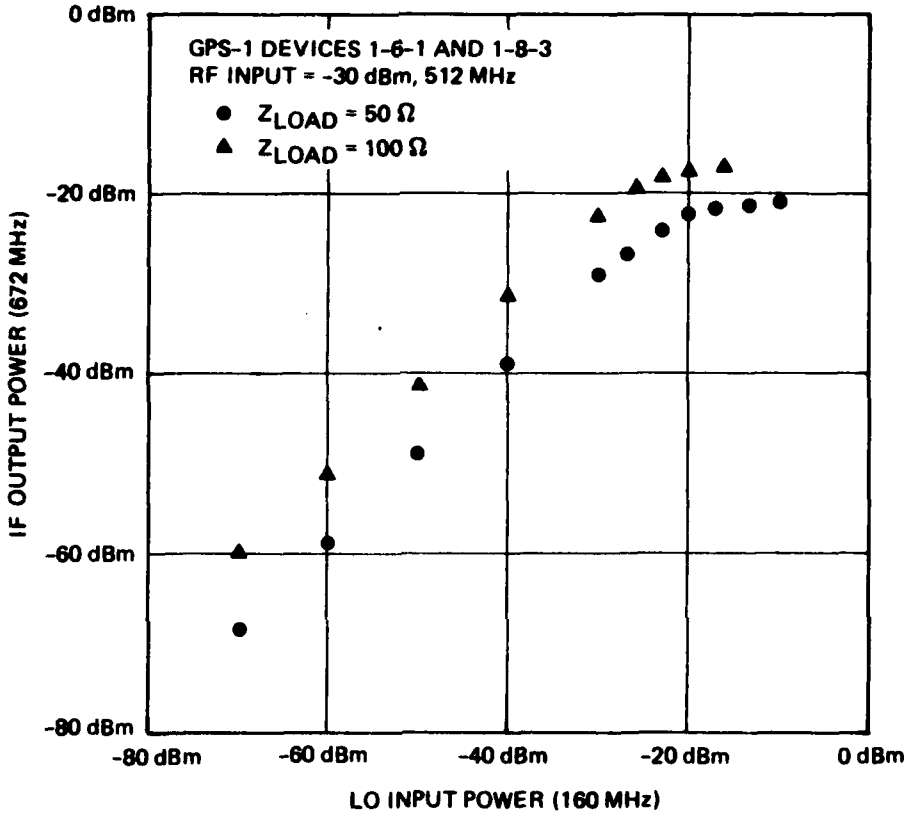


Figure (6.5). GPS Analog Multiplier Output Compression at 672 MHz.

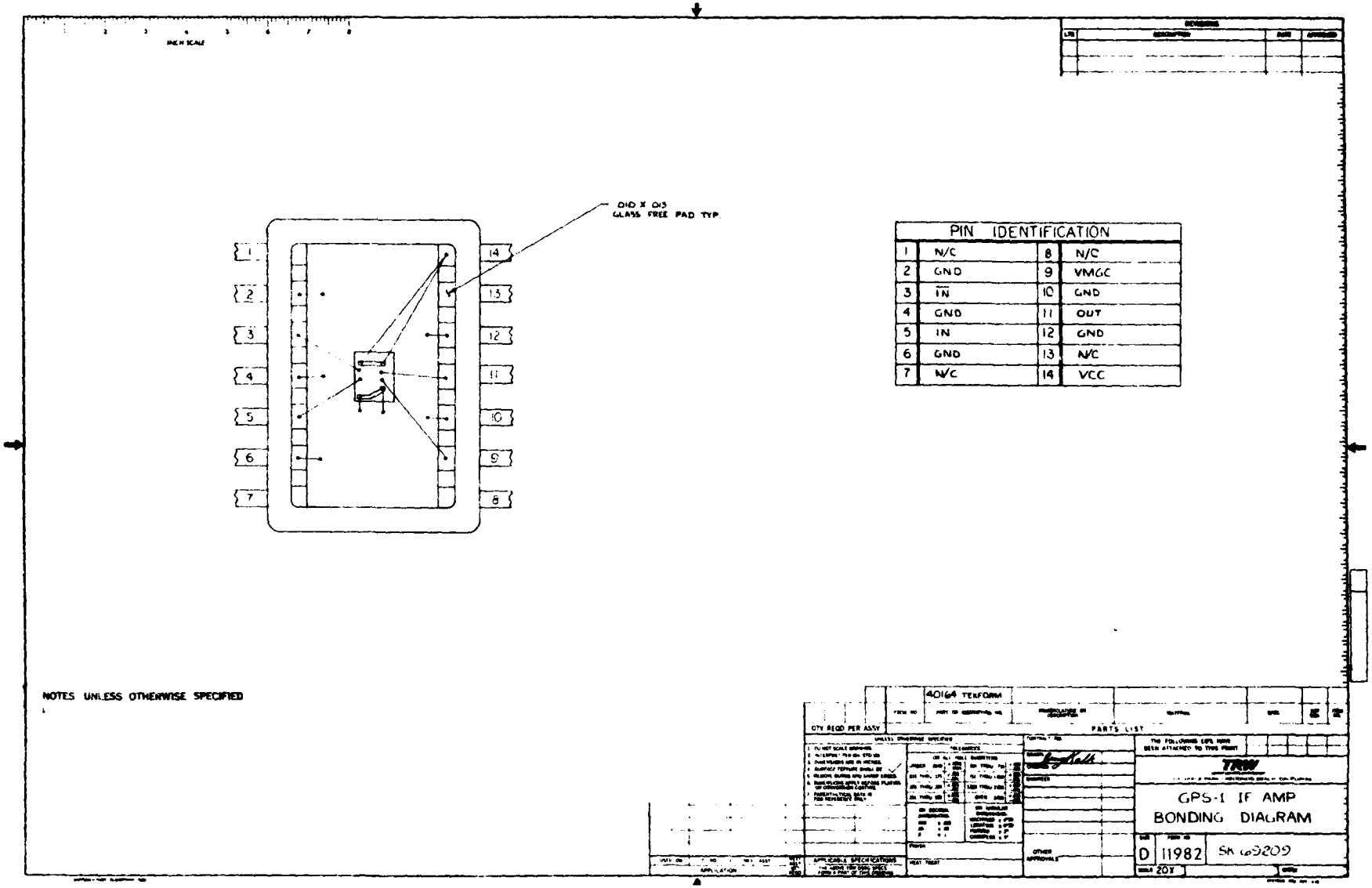
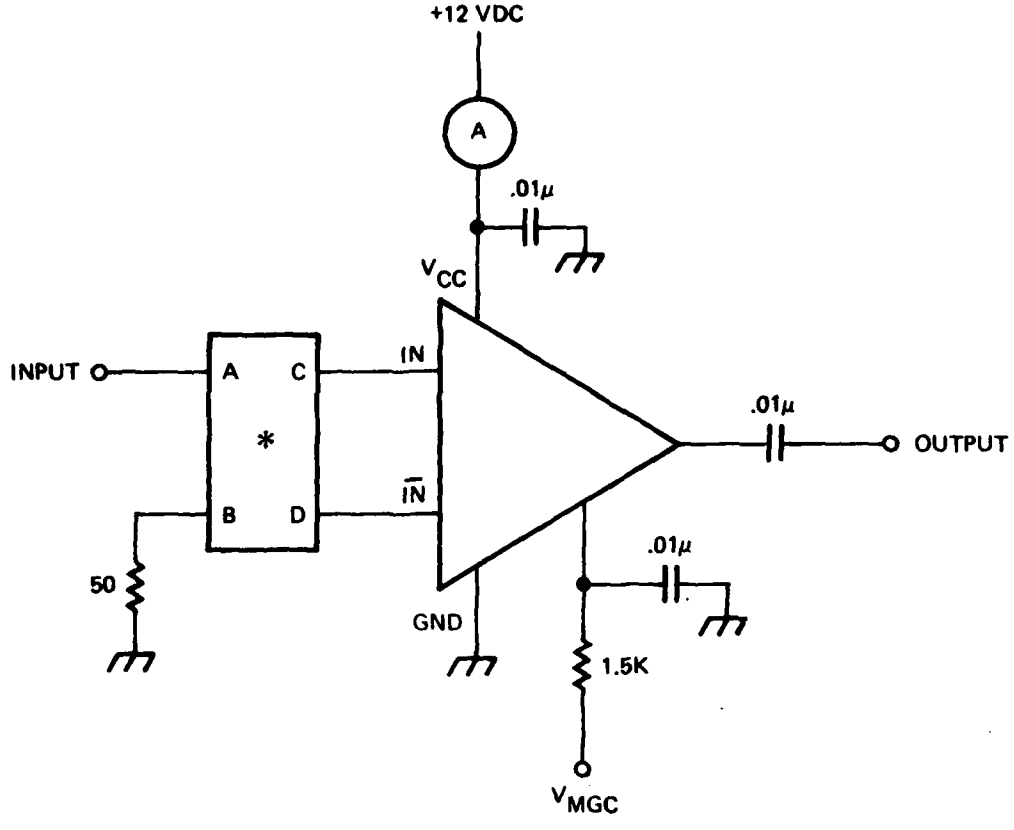


Figure (6.6). GPS IF Amplifier Test Package Diagram.



NOTES:
1. INPUT SUPPLIED BY HP 8660C/86603A SIGNAL GENERATOR.
2. V_{MGC} LEFT OPEN CIRCUITED FOR NOMINAL OPERATION.

Figure (6.7). GPS IF Amplifier Test Circuit.

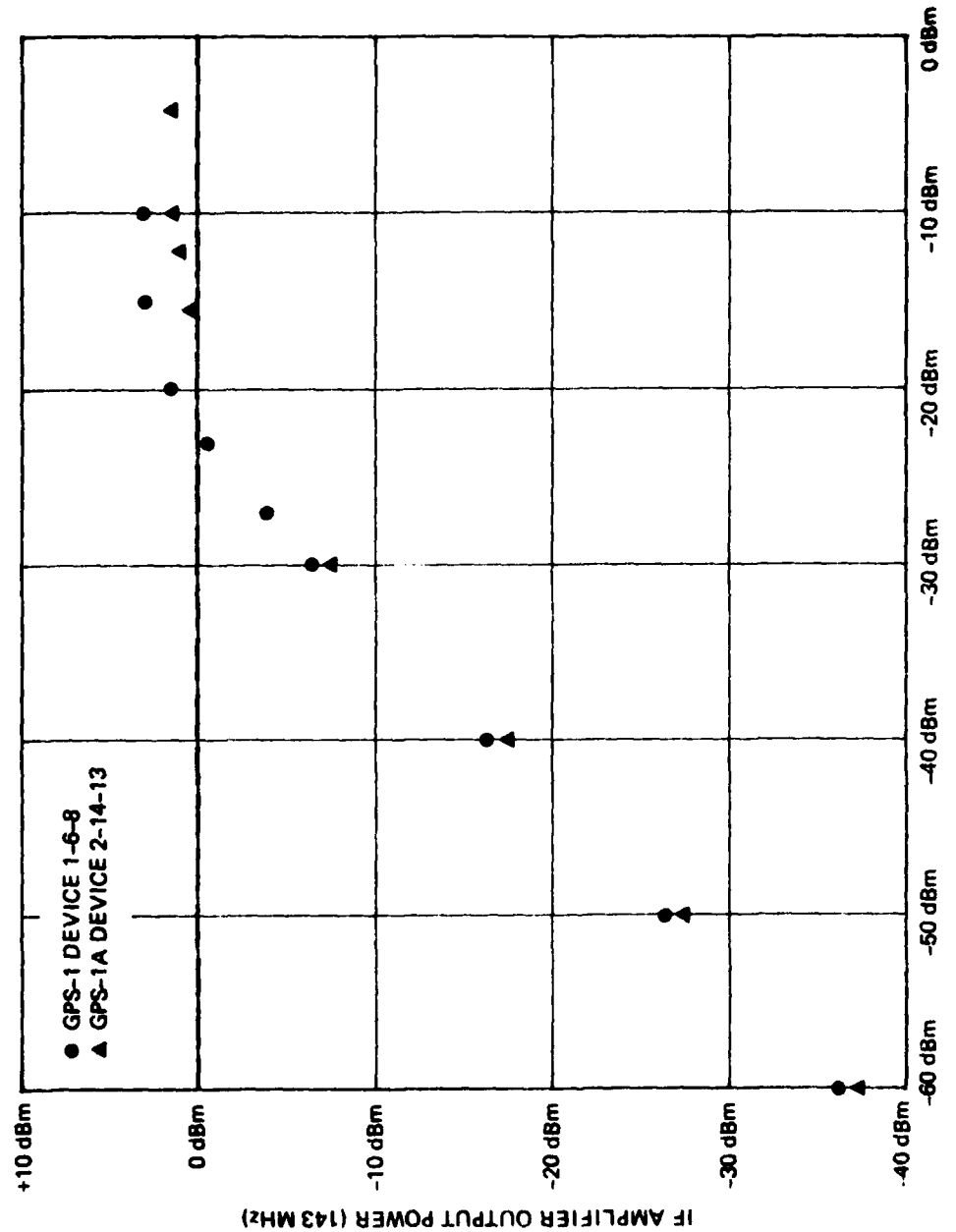


Figure (6.8). GPS IF Amplifier Output Compression at 143 MHz.

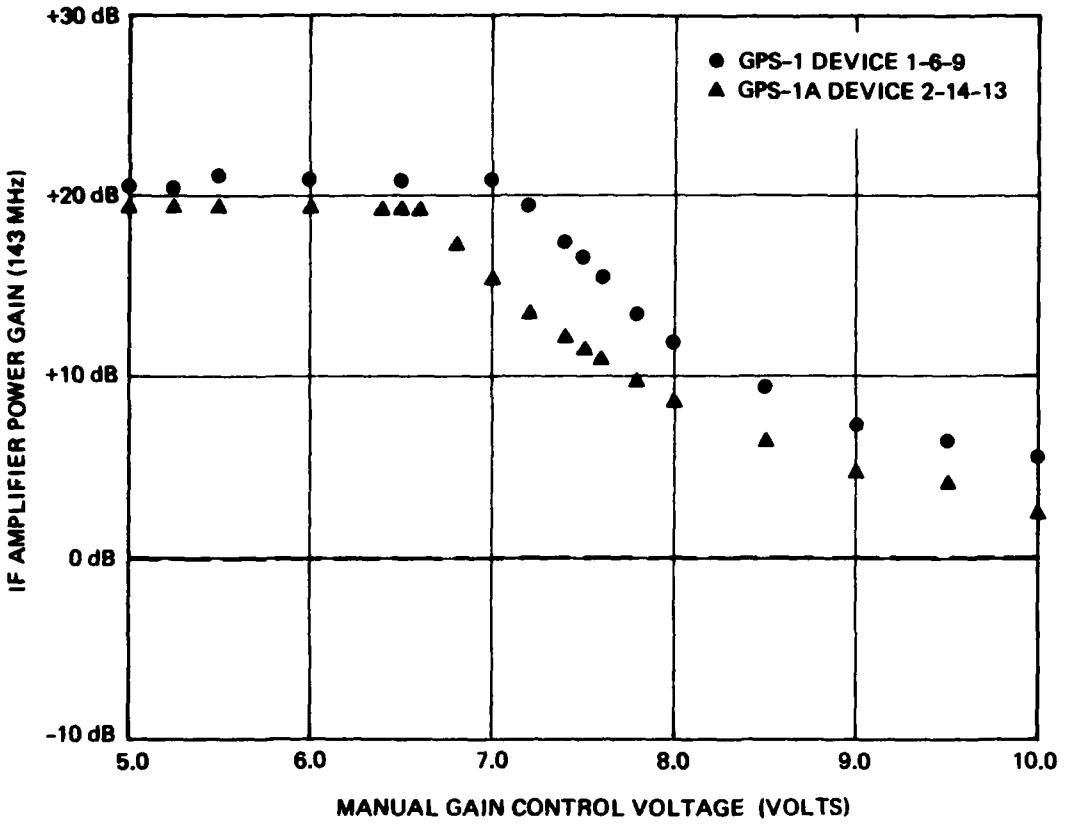


Figure (6.9). GPS IF Amplifier Gain at 143 MHz as a Function of MGC Voltage.

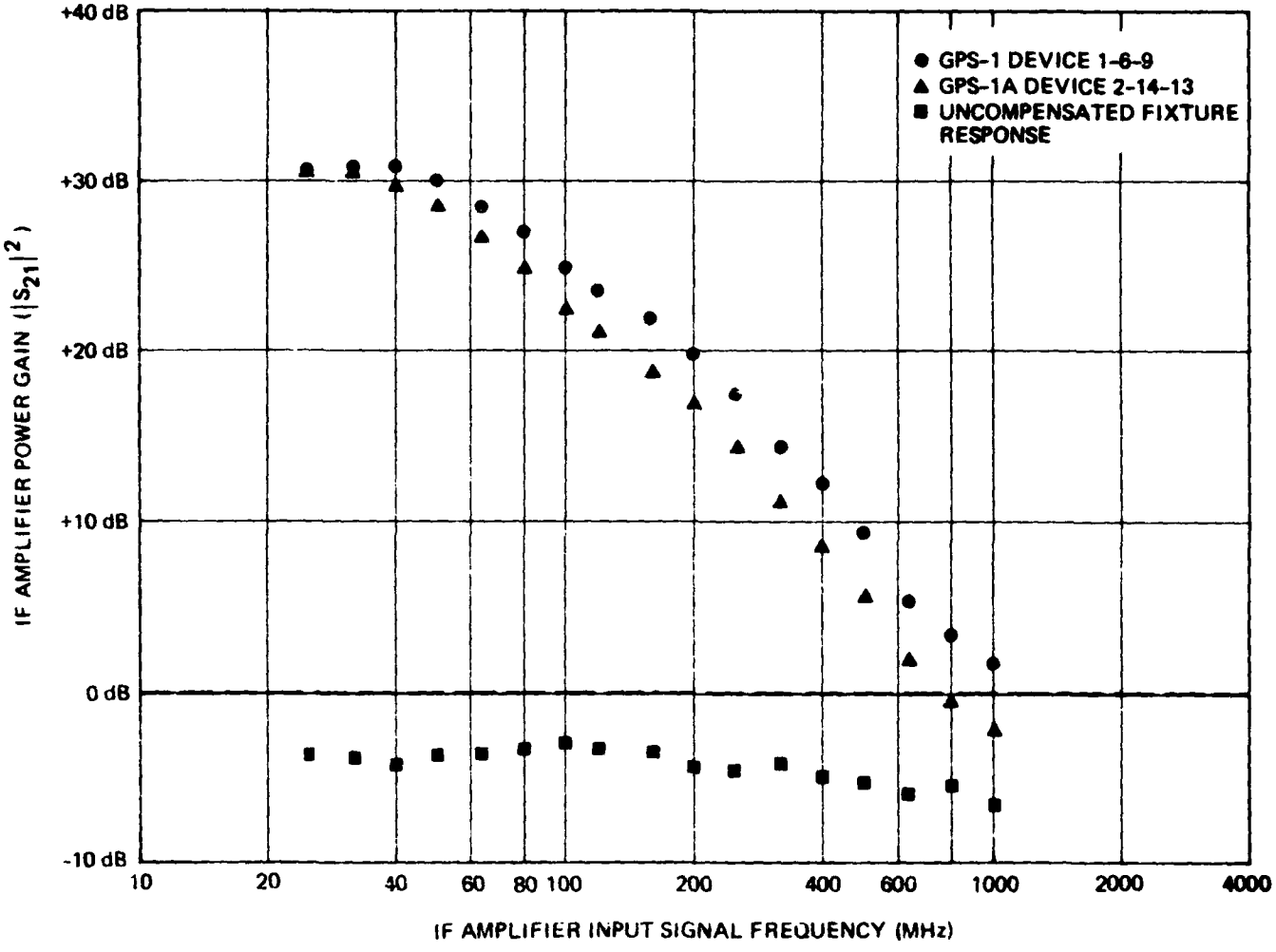


Figure (6.10). GPS IF Amplifier Gain as a Function of Frequency (Vector Voltmeter)

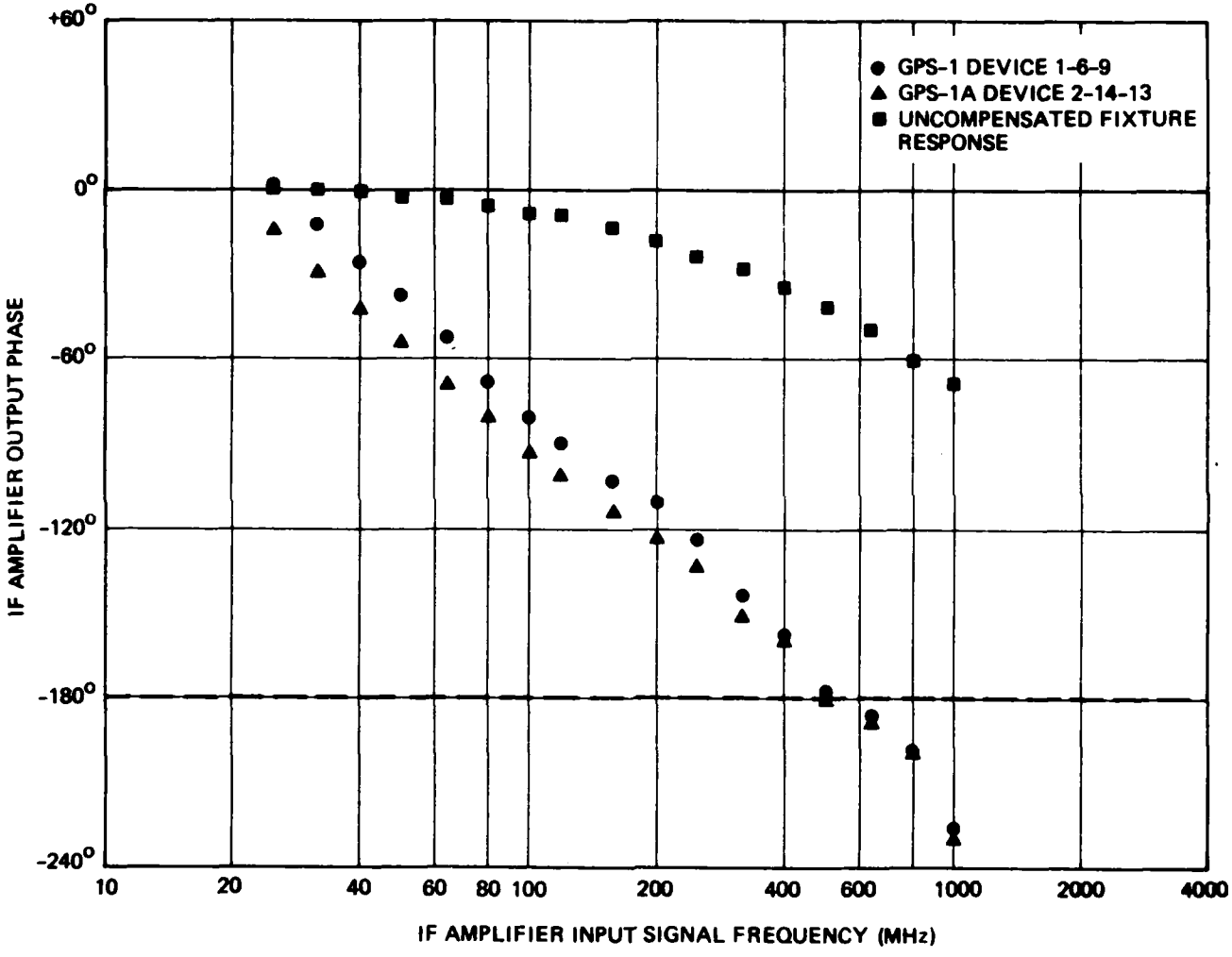


Figure (6.11). GPS IF Amplifier Output Phase as a Function of Frequency (Vector Voltmeter).

pole, but the continued high frequency roll-off suggests another multiple pole just above 1 GHz. The test fixture calibration data, which was used to correct the device measurements, are also shown in figures (6.10) and (6.11).

6.2.4 RF Amplifier

The GPS RF test amplifier chips were packaged for electrical characterization as shown in figure (6.12). A test fixture was constructed to implement the circuit shown in figure (6.13). Eighteen chips from three wafers were screened for bias supply power dissipation and for power gain at 1575 MHz. Five samples were then selected for detailed characterization.

RF amplifier power gain at 1575 MHz for two sample devices is shown as a function of AGC voltage in figure (6.14). The gain decrease is seen to be gradual for AGC levels less than 0.6V where a sharp increase in sensitivity occurs.

The variation of amplifier power gain with frequency is shown for three sample devices in figure (6.15). (The GPS-1 sample was biased at a lower V_{CC} voltage to prevent burnout of a sensitive first-stage resistor, a problem that was corrected in the GPS-1A devices.) The key features of the RF amplifier gain-frequency curve are the quadruple-zero low frequency roll-off, the underdamped double-pole break at midband, and the sharp high frequency roll-off.

6.2.5 LO Buffer

The GPS LO buffers were packaged for characterization as shown in figure (6.16) and tested in the circuit given in figure (6.17). Four devices were selected for characterization from a total of eight packaged chips.

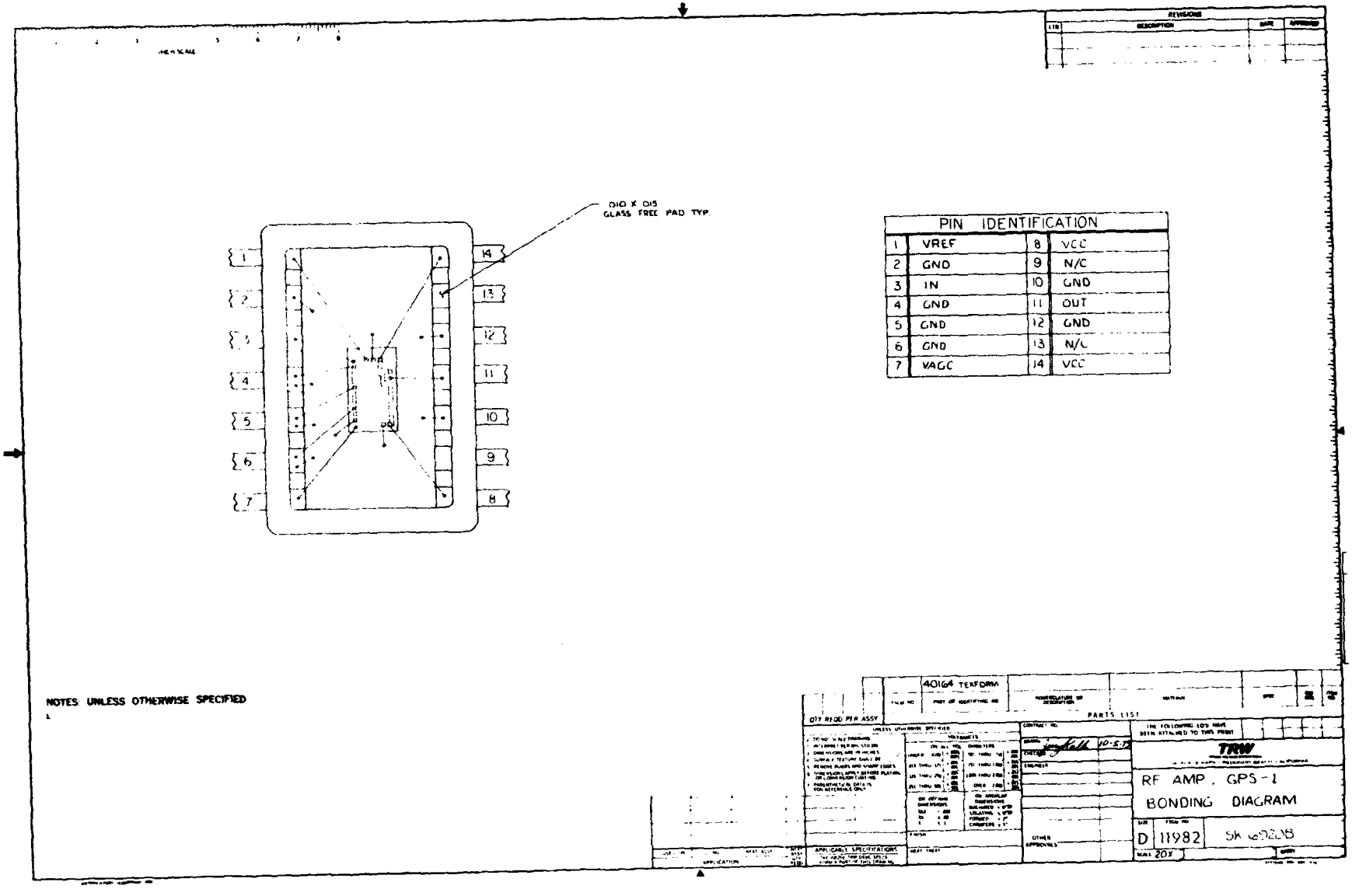
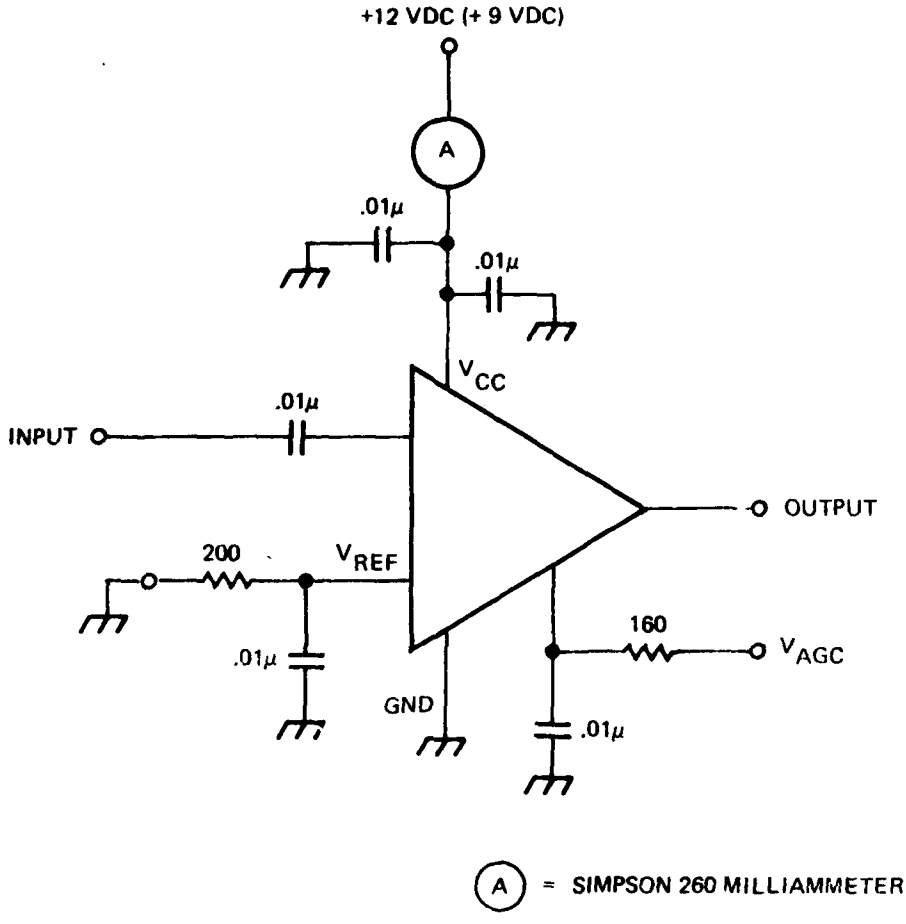


Figure (6.12). GPS RF Amplifier Test Package Diagram.



NOTES:
1. INPUT SUPPLIED BY HP 8660C/86603A SIGNAL GENERATOR.
2. V_{AGC} SET TO 0 VDC (GROUNDED) FOR NOMINAL OPERATION.
3. V_{CC} SET AT +12 VDC FOR GPS-1A, +9 VDC FOR GPS-1.

Figure (6.13). GPS RF Amplifier Test Circuit.

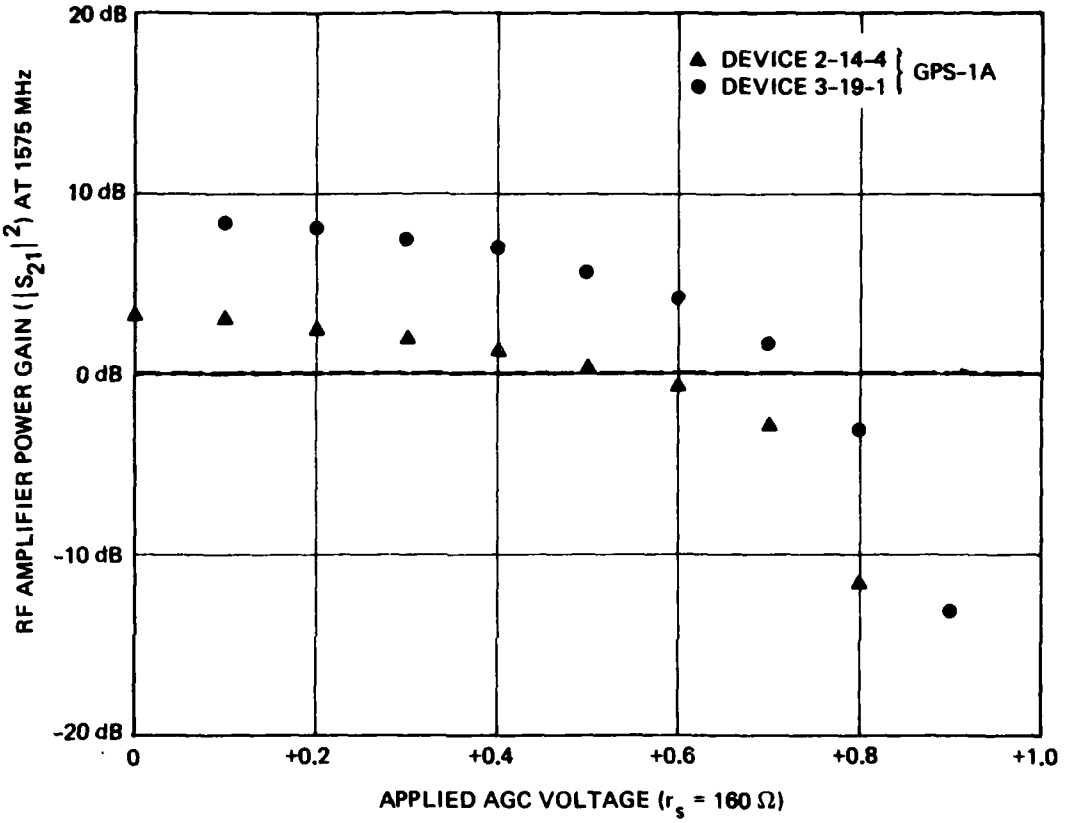


Figure (6.14). GPS RF Amplifier Gain at 1575 MHz as a Function of AGC Voltage.

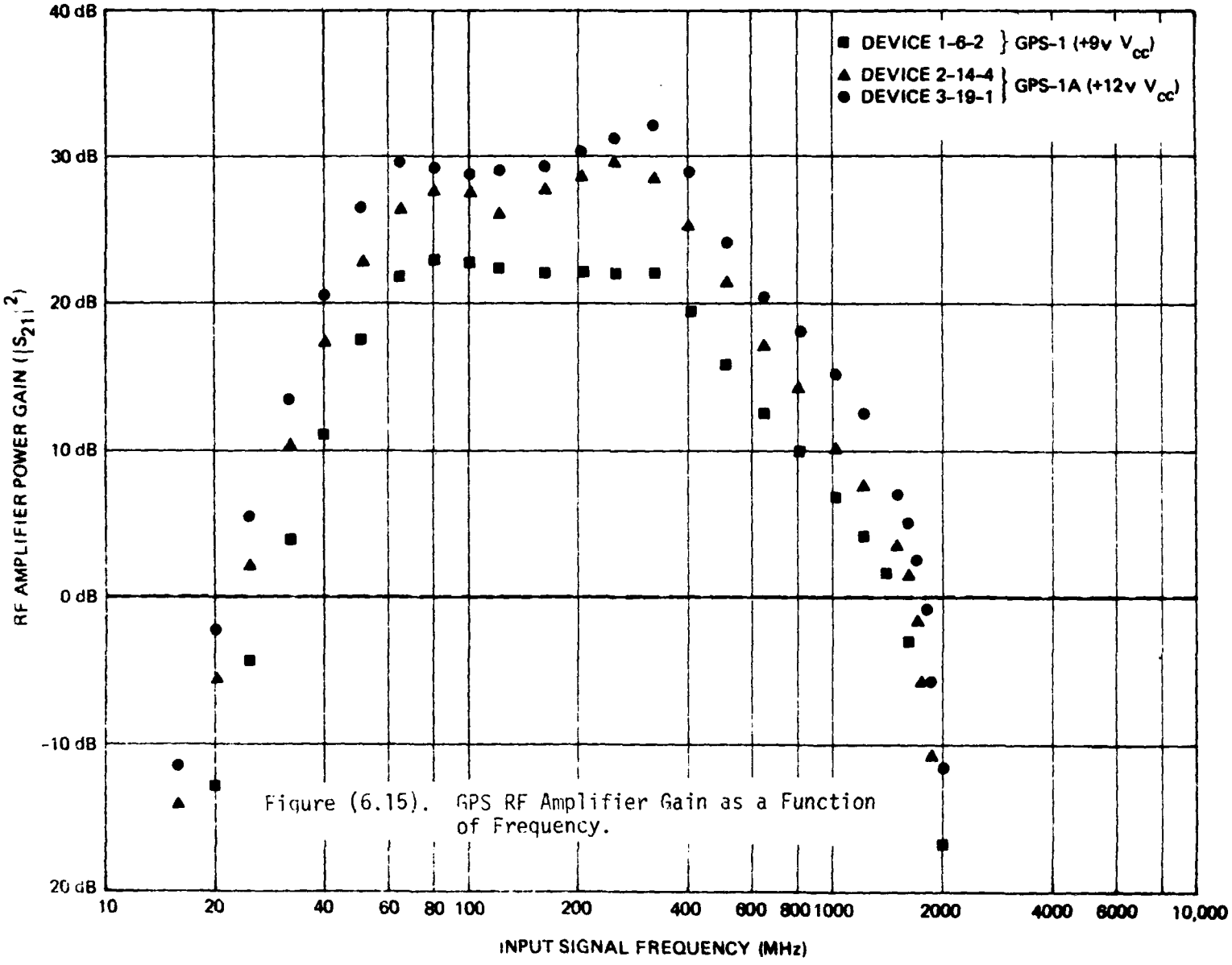


Figure (6.15). GPS RF Amplifier Gain as a Function of Frequency.

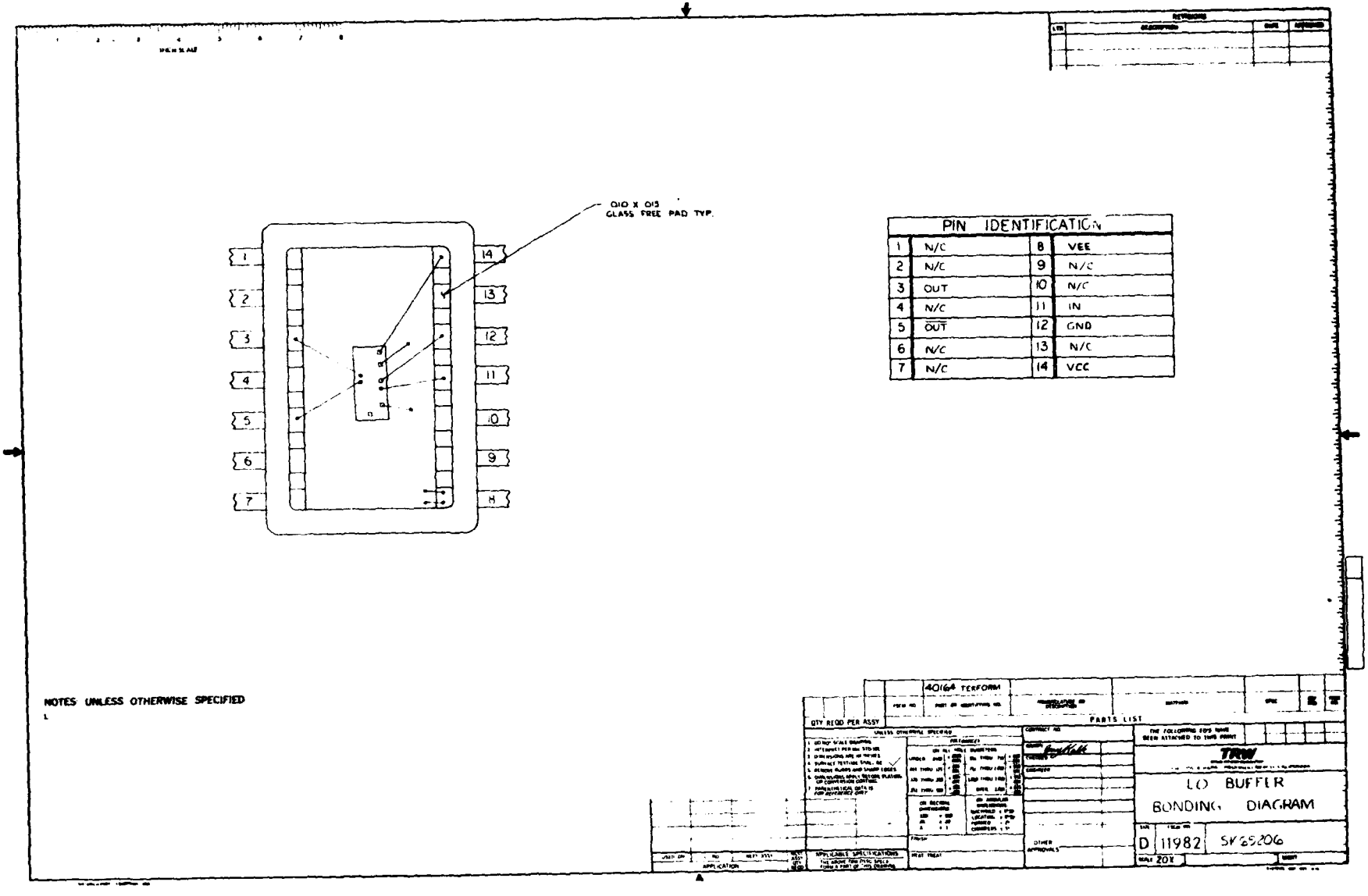
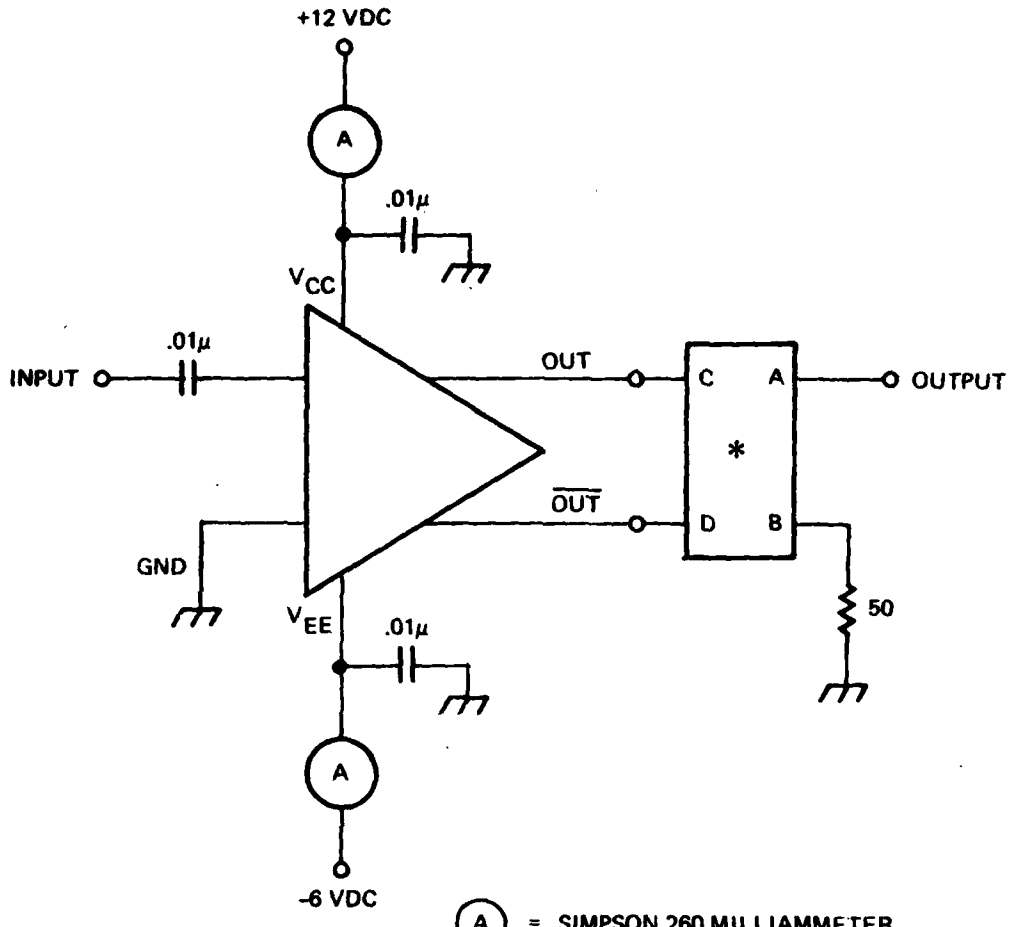


Figure (6.16). GPS LO Buffer Test Package Diagram.



NOTES:
1. INPUT SUPPLIED BY HP8660C/86603A SIGNAL GENERATOR.
2. ALTERNATE METHOD OF OUTPUT MEASUREMENT IS TO MONITOR ONE TERMINAL DIRECTLY AND TERMINATE OTHER WITH 50 Ω TO GROUND.

Figure (6.17). GPS LO Buffer Test Circuit.

A plot of LO Buffer output power as a function of input power at 1432 MHz for two selected devices is given in figure (6.18). The data indicate close agreement in the performance of the two devices and show linear operation to the 1 dB compression point at -7 dBm input power.

LO Buffer power gain as a function of frequency is displayed in figure (6.19) for two devices. The data indicate a broad flat-gain region with a high frequency double pole roll-off dominating above 600 MHz.

6.2.6 GPS System

The dice containing the complete GPS system electronics were packaged for preliminary characterization as shown in figure (6.20). The devices were tested with the circuit shown in figure (6.21). The package and fixture were designed to test only the down-conversion circuits of the system chip; to this end, the digital inputs and the code tracking circuit connections were defaulted in the test package. A total of fourteen system chips were screened; two of those found functional were then characterized.

The down-conversion subsystem was treated as a simple analog multiplier; performance was evaluated in terms of a gain factor k ($= P_{IF}/P_{LO}P_{RF}$). However, the noisy and nonlinear behavior of the system chip made single point data unreliable. Therefore, a minimum of four combinations of input LO and RF power levels were used at each frequency to characterize the IF output gain factor.

The GPS system gain factor for one sample device is shown in figure (6.22) as a function of varying RF input frequency with a constant IF output frequency of 143 MHz. The data show considerable scatter at lower frequencies. However, the well-defined min/max peaking at 1500 MHz suggests that the low frequency scatter may be due to actual circuit resonance phonomena. Such resonance behavior might arise from energy coupling internal to the chip between the down-conversion subsystem and the various code input and tracking circuits.

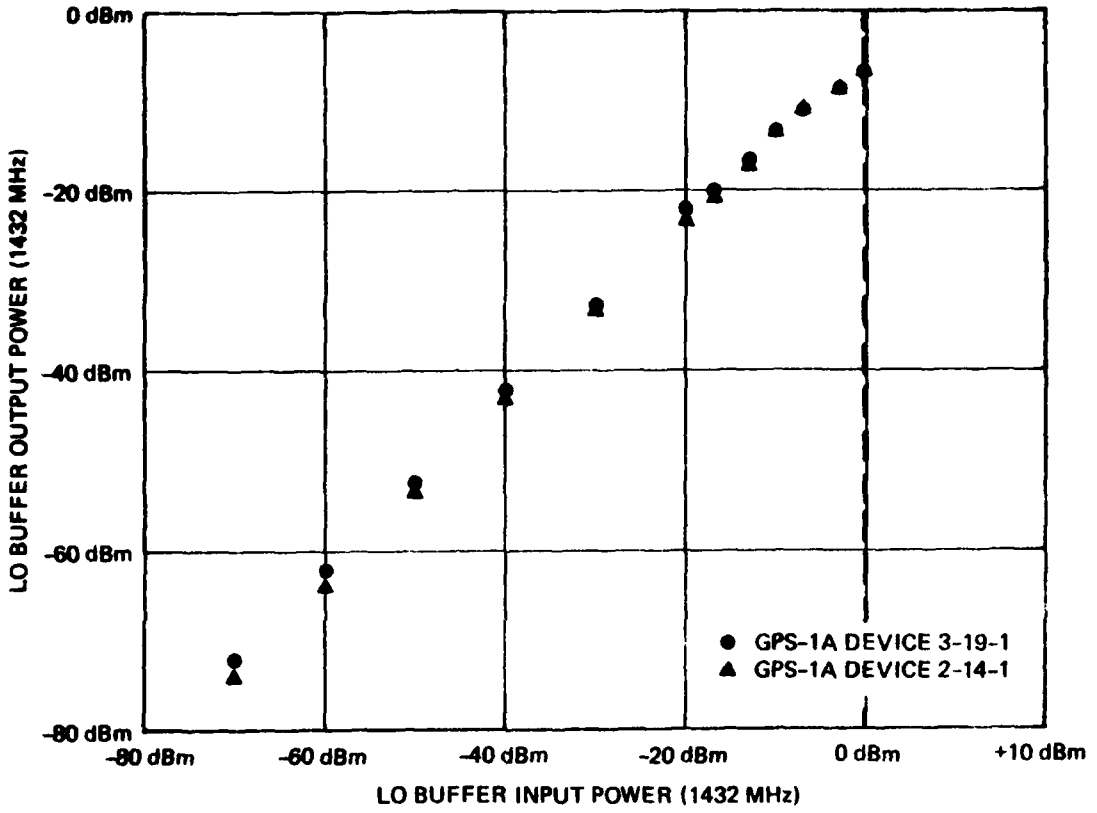


Figure (6.18). GPS LO Buffer Output Compression at 1432 MHz.

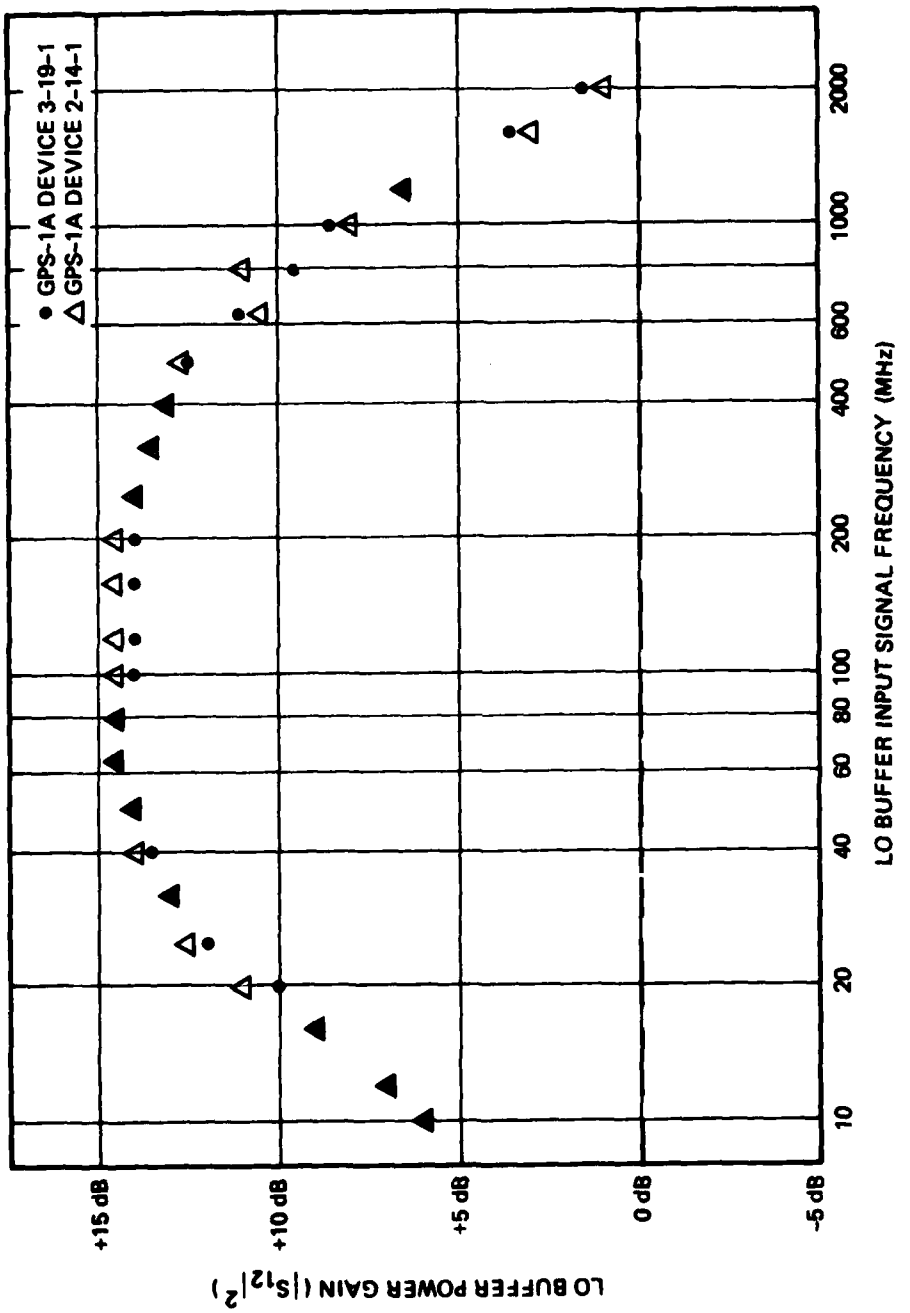


Figure (6.19). GPS LO Buffer Gain as a Function of Frequency.

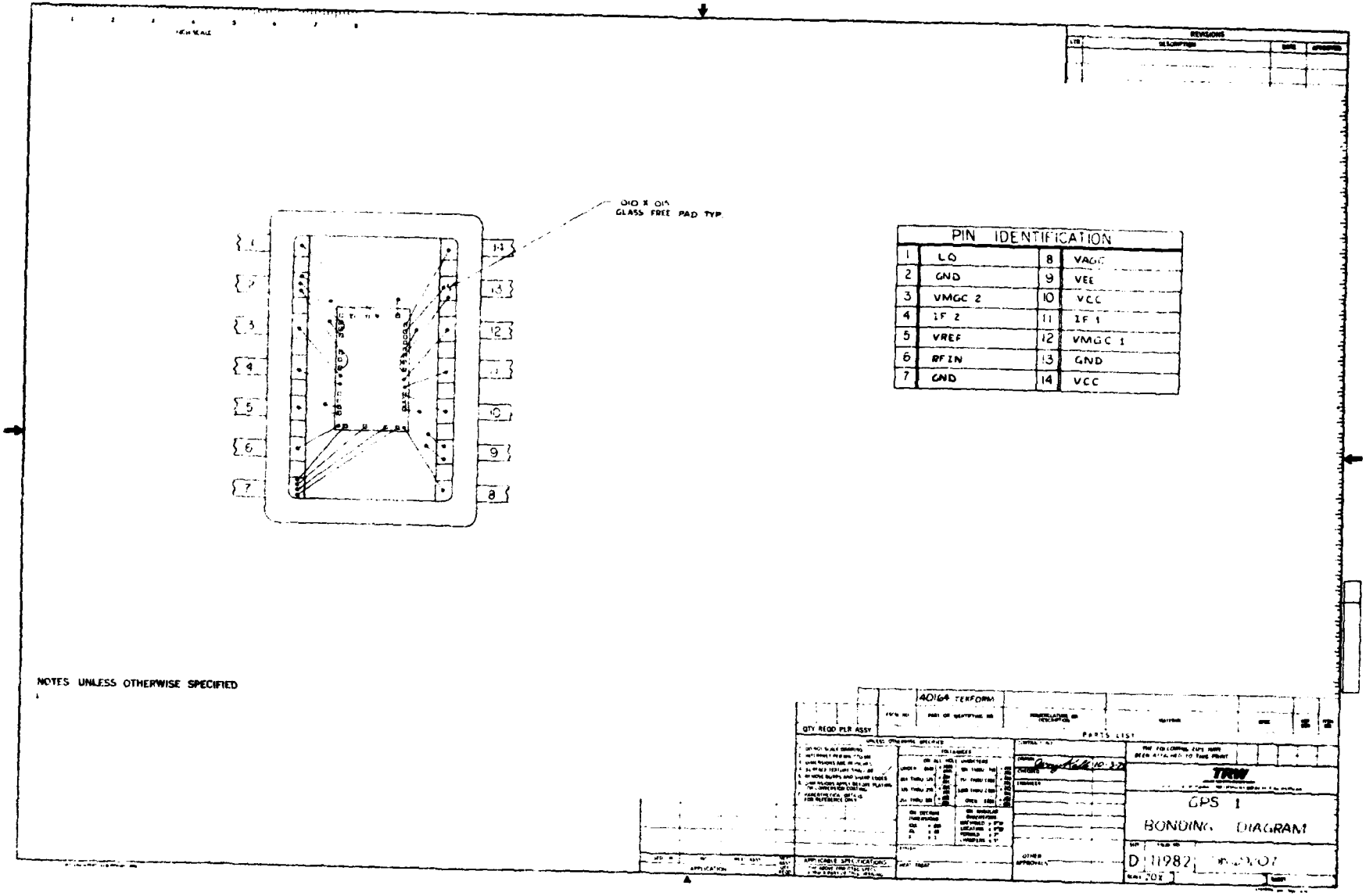
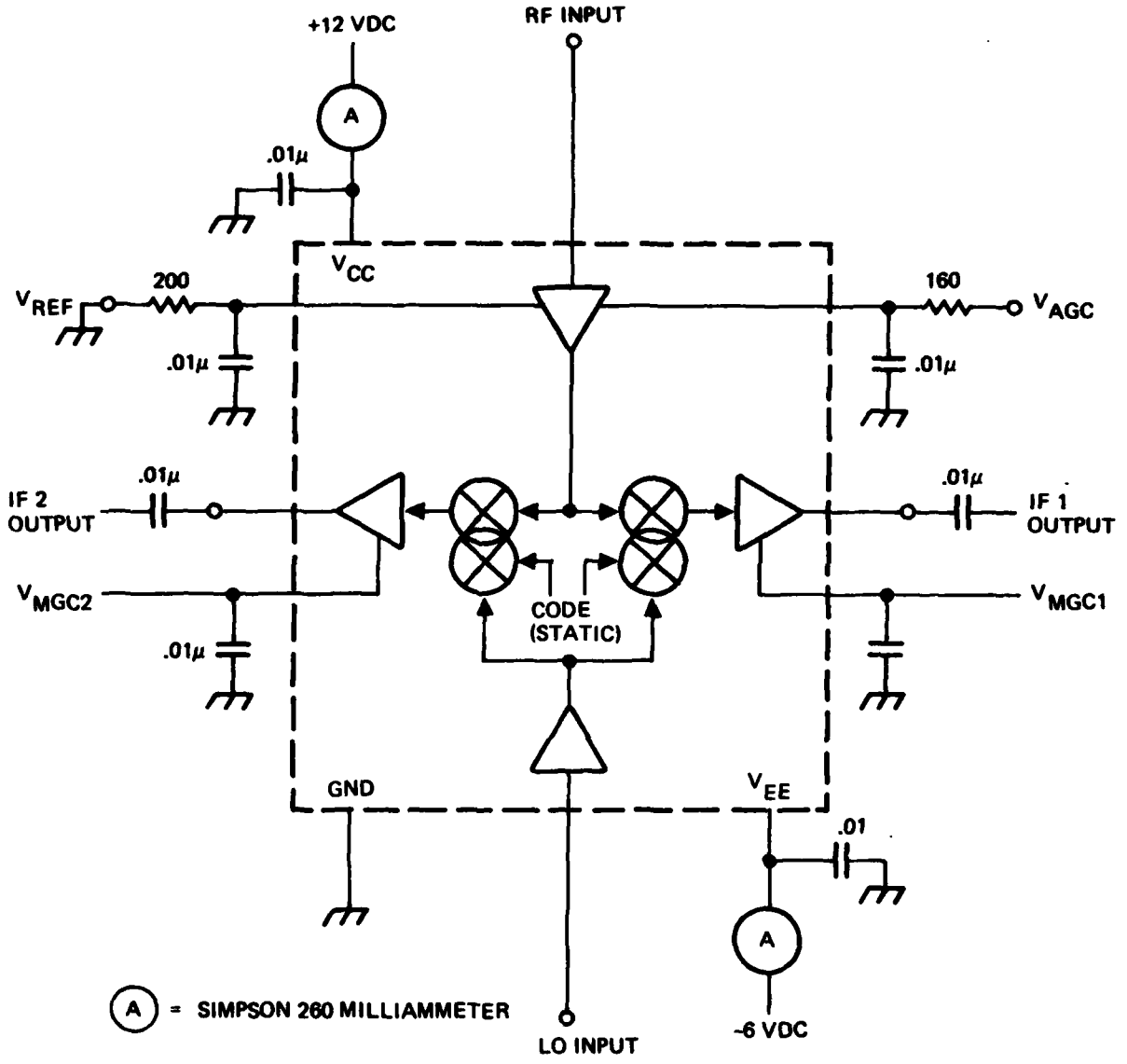


Figure (6.20). GPS System Chip Test Package Diagram.



NOTES:

1. ONE OUTPUT MONITORED WITH SPECTRUM ANALYZER (HP141T/8555A/8552B); UNUSED OUTPUT TERMINATED WITH 50 Ω TO GROUND.
2. CONTROL VOLTAGES FOR NOMINAL OPERATION ARE V_{REF} = 0V, V_{AGC} = 0V, V_{MGC1} AND V_{MGC2} OPEN.
3. DIGITAL CIRCUITRY BYPASSED TO PROVIDE AN UNCHANGING CODE INPUT TO MIXERS.

Figure (6.21). GPS System Chip Test Circuit

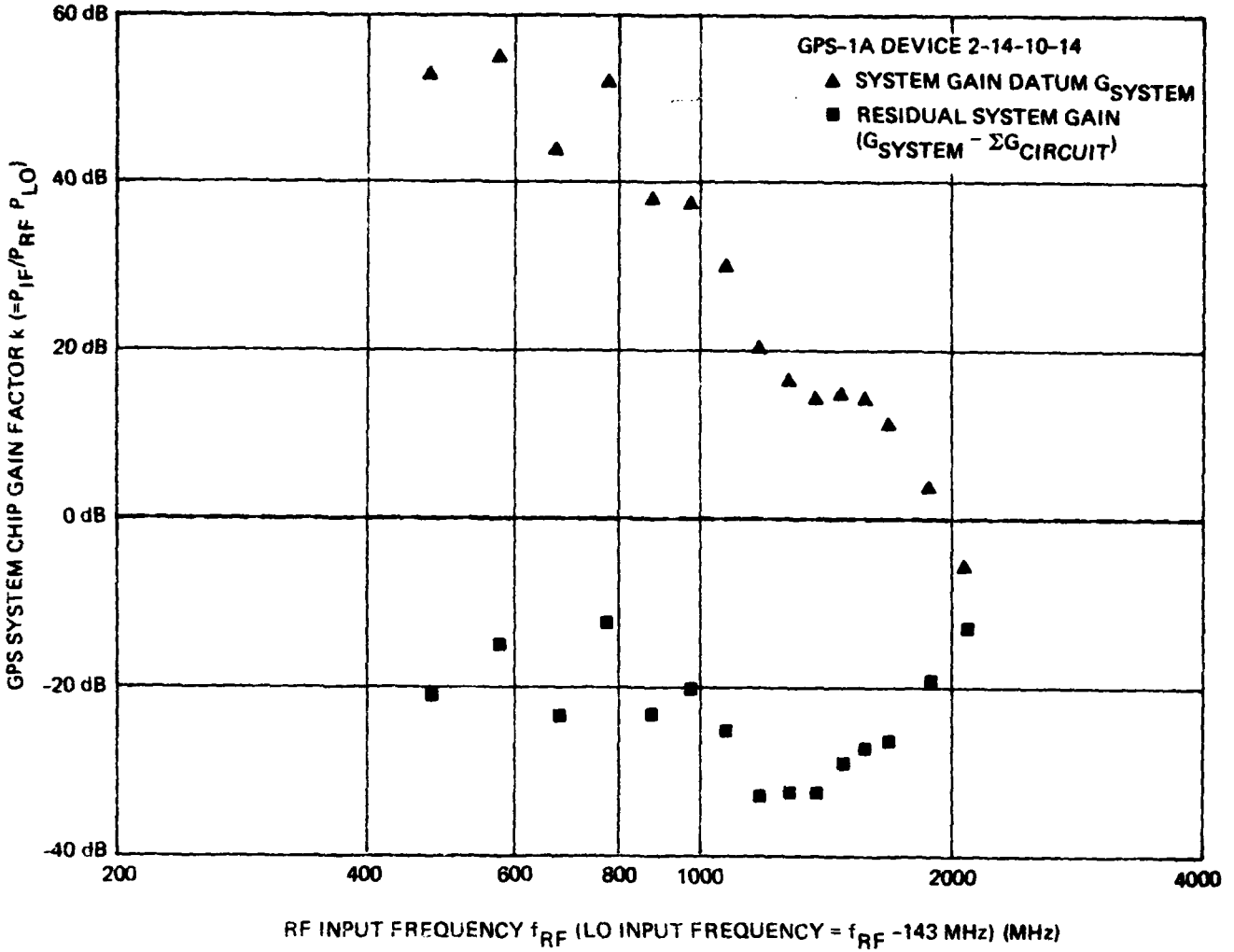


Figure (6.22). GPS System Chip Gain Factor as a Function of Input Frequency.

The system residual gain, defined as the difference between the measured system gain and the linear combination of the gains measured for each of the constituent circuits, is also displayed in figure (6.22). It was expected that the monolithic interconnection of the system elements would be more efficient because of the designed close impedance matching between circuits. The fact that the residual gain data average -23.5 dB with no data greater than -10 dB indicates that either the interelement coupling is remarkably inefficient or that the individual circuits themselves are markedly different in the system chip from the separate test chips.

6.3 Conclusions (GPS Circuit Characterization)

Although the test results reported here are preliminary, the following conclusions can be made.

a. The GPS analog multiplier does not meet the design goal gain factor requirement (20 dB at P_{LO} = -25 dBm); there is sufficient gain at lower frequencies but the effective bandwidth of the device limits available gain at the design nominal frequency.

b. The GPS IF and RF amplifiers do not meet the design goal gain requirements (MGC variable -13 dB to 28 dB for the IF, AGC variable 15 dB to 30 dB for the RF); both amplifiers have sufficient gain at lower frequencies but are limited by effective bandwidth at the design nominal frequencies.

c. The GPS LO buffer circuit meets the design goal gain requirement.

d. The GPS system chip RF-IF signal path is functional; however, more testing is required for characterization.

7.0 CONCLUSIONS

The second year of contractual effort has witnessed substantial technical maturation with respect to the application of advanced circuit theory to the problem of accurately predicting integrated circuit performance in advance of fabrication. Definitive manual analyses, complemented with extensive and prudent use of computer simulation tools, have become implicit components of the RFLSI design process. These analytical efforts have resulted in markedly enhanced understanding of both parasitic and purposefully induced signal flow patterns within an integrated circuit and in turn, this understanding has precipitated an ability to predict actual high frequency circuit performance with greatly increased accuracy. Errors rarely exceed 15%.

A second technical area that has undergone considerable strengthening in the past year has been circuit testing and evaluation. RFLSI circuits presently undergo what might be termed "corroborative" evaluation; that is, circuit performance is never measured by only one method but rather, it is ascertained by way of two, and often three or four, independent measurement techniques. This assiduous characterization procedure, coupled with data analyses whose level of sophistication closely parallels that of the analyses performed during the initial circuit design cycle, has often succeeded in properly identifying parasitic signal flow paths on chip that might otherwise have been erroneously discounted or completely overlooked. As a result, testing is no longer viewed as a separate technical discipline but instead, the lessons learned as a consequence of its ramifications are explicitly factored into the design cycle.

Finally, the active peaking concept, disclosed in theoretical terms during the first year of effort, has been successfully implemented in both the RF and IF amplifiers embedded in RFCS-1. The concept spells efficient and even aesthetically satisfying wideband and narrowband analog RFLSI design, since it all but completely abrogates the necessity

to incorporate on-chip spiral inductors. Spiral inductors consume inordinately large chip area and, as confirmed by GPS and GPS1A testing, they are particularly troublesome because of the parasitic susceptive coupling they incur to the substrate.

7.1 Present Status

The technical status of contractual endeavors as of 1 October 1979 is briefly overviewed below.

(1) The GPS1 and GPS1A test chips have been fully characterized. Their performance has been found to be poor due to low RF amplifier gain and the presence of spurious frequencies within the code tracking loop. The RF amplifier gain is low due to inappropriate interstage matching incurred as a result of ostensibly uncontrollable on-chip inductor parasitics. Code tracking loop oscillations are present in most GPS1A chips due to an improperly stabilized operational amplifier.

(2) RFCS-1 is undergoing test and evaluation. Preliminary results portend excellent RF and IF amplifier performance which closely tracks with analytical predictions documented at the conclusion of the circuit design phase.

(3) A Costas Loop demodulator is undergoing design as are stand-alone operational amplifier and stand-alone analog multiplier building blocks.

(4) The possibility of configuring a receiver breadboard is being explored as a means of unequivocably establishing bipolar RFLSI as a viable technology for processing analog signals whose frequencies span L-band.

7.2 Future Work

The primary areas of concern that are to be addressed during the final contract phase are advanced circuit concepts and realization of stand-alone RFLSI building block circuits that are suitable for use in a broad variety of electronic system applications. The advanced circuit concepts derive in part from the following list of subject areas.

(1) Improved wideband amplifier performance through optimized sampled frequency device characterization.

(2) Further exploration of controlled negative resistance gain cells as a means of achieving an effective multiplication of device gain-bandwidth product.

(3) Efficient factorization of low distortion and low noise requirements into RF and IF amplifier design procedures.

(4) Investigation of the realizability of high Q active inductor circuits and floating active inductors by means of Darlington synthesis and network gyration.

(5) Improved device and circuit modeling by implementing parameter extraction procedures that implicitly incorporate test data, fundamental processing characteristics, and circuit layout topology.

(6) Enhancing circuit testability through designs that ensure minimal voltage standing wave ratio (VSWR) with respect to a 50 ohm reference impedance.

Operational amplifiers, four-quadrant analog multipliers, RF and IF active filters, and general-purpose RF and IF amplifiers are prime initial candidates for implementation as stand-alone building blocks. The potential success achieved in this implementation task is strongly a function of the success experienced in positively addressing the foregoing six advanced circuit concepts, particularly subject areas one through four.

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